RCV336ACF/SP and RCV144ACF/SP Modem Device

Designer's Guide (Preliminary)

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Rev. 3, August 2, 1996

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1. INTRODUCTION

1.1 SUMMARY

The Rockwell RCV336ACF/SP and RCV144ACF/SP Modem Device Families support high speed data, high speed fax, AudioSpan, speakerphone, voice/audio, and VoiceView operation. They are intended for use with dial-up telephone lines in the U.S. or world-wide and are eacg family is offered in six device models (Table 1-1).

The RCV336ACF/SP supports data line rates to 33.6 kbps in data modem mode or data line rates from 4.8 to 14.4 kbps plus audio in AudioSpan mode; the RCV144ACF/SP supports data line rates to 14.4 kbps in data modem mode or data line rates from 4.8 to 9.6 kbps plus audio in AudioSpan mode;

These RCV336ACF/SP and RCV144ACF/SP F-class modem devices are pin compatible, allowing design of a common printed circuit board to support either V.34 or V.32 bis modem performance, respectively, with the only hardware difference being the installed modem device.

Analog simultaneous audio/voice and data (AudioSpan) operation supports data rates with audio of 4.8 kbps in V.61 modulation or 4.8 to 9.6 kbps in ML144 modulation. The RC336/RCV336 also supports data rates with audio of 4.8 to 14.4 kbps in ML288 modulation.

SP models support position-independent, full-duplex speakerphone (FDSP).

As a data modem, the modem operates at line speeds to 33600 bps. Error correction (V.42/MNP 2-4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost average data throughput up to 115.2 kbps. Non-error-correcting mode is also supported.

Error correction and data compression (ECC) is performed in the modem using 32k bytes of external RAM to increase data throughput typically by a factor of four.

The modem supports fax Group 3 send and receive rates up to 14400 bps and supports T.30 protocol.

In voice/audio mode, enhanced ADPCM coding and decoding supports efficient digital storage of voice/audio using 2-bit or 4-bit per sample compression and decompression with a 7200 Hz sample rate. This mode also supports 8-bit monophonic audio encoding at 11.025 kHz or 7200 Hz. This mode supports digital telephone answering machine (DTAM), voice annotation, and audio recording and playback applications.

The modem device is packaged in a 68-pin PLCC.

Reference hardware designs are available with and without interface to sound chips (audio codecs). Voice/audio designs support functions such as music on hold and telephone/speakerphone conversation recording.

PC-based "ConfigurACE™ II for Windows" software allows modem firmware to be customized to application and country requirements. ConfigurACE™ II for Windows operation and programmable country call progress parameters are described in the on-line documentation accompanying the software.

This designer's guide describes the modem hardware capabilities and identifies the supporting AT commands. AT commands and S Registers are defined in the AT Command Reference Manual (Order No. 1048).

Table 1-1. Modem Models and Functions

Model	Supported Functions				
	Data/Fax	AudioSpan	FDSP	Voice/Audio VoiceView	W-Class
RCV336ACF/SP	V.34/V.17	V.61/ML144/ML288	S	S	-
RCV336ACFW/SP	V.34/V.17	V.61/ML144/ML288	S	S	S
RCV336ACF	V.34/V.17	V.61/ML144/ML288	-	S	-
RCV336ACFW	V.34/V.17	V.61/ML144/ML288	-	S	S
RC336ACF	V.34/V.17	V.61/ML144/ML288	-	-	-
RC336ACFW	V.34/V.17	V.61/ML144/ML288	-	-	S
RCV144ACF/SP	V.32 bis/V.17	V.61/ML144	S	S	-
RCV144ACFW/SP	V.32 bis/V.17	V.61/ML144	S	S	S
RCV144ACF	V.32 bis/V.17	V.61/ML144	-	S	-
RCV144ACFW	V.32 bis/V.17	V.61/ML144	-	S	S
RC144ACF	V.32 bis/V.17	V.61/ML144	-	-	-
RC144ACFW	V.32 bis/V.17	V.61/ML144	-	-	S

Notes:

1. Model options:
   - SP — Speakerphone.
   - V — Voice, audio, and VoiceView.
   - W — World-class (W-class).
2. Supported functions (S = Supported; – = Not supported):
   - AudioSpan — Analog simultaneous audio/voice and data.
   - FDSP — Full-duplex speakerphone.
   - Voice/audio — Voice and audio functions.
   - VoiceView — VoiceView alternating voice and data.
   - W-Class — World-class functions supporting multiple country requirements.

1.2 FEATURES

- AudioSpan (simultaneous audio/voice and data)
  - ITU-T V.61 modulation (4.8 kbps data plus audio)
  - ML144 modulation (4.8 to 9.6 kbps data plus audio)
  - ML288 modulation (4.8 to 14.4 kbps data plus audio)
  - Audio/silence detection (ML144) and handset echo cancellation
  - Handset, headset, or half-duplex speakerphone
- Full-duplex speakerphone (FDSP) mode (option)
  - Acoustic and line echo cancellation
  - Microphone gain and muting
  - Speaker volume control and muting
  - Room monitor
- Data modem throughput up to 115.2 kbps
  - 33.6 kbps and V.34 (RCV336 only)
  - V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103
  - V.42 LAPM, MNP 2-4, and MNP 10 error correction
  - V.42 bis and MNP 5 data compression
  - MNP 10EC™ enhanced cellular performance
  - Hayes AutoSync (option)
- Fax modem send and receive rates up to 14400 bps
  - V.33, V.17, V.29, V.27 ter, and V.21 channel 2
- Voice/audio mode (option)
  - Enhanced ADPCM compression/decompression
  - Tone detection/generation and call discrimination
  - Concurrent DTMF detection
  - 8-bit monophonic audio data encoding at 11.025 kHz or 7200 Hz
- VoiceView alternating voice and data (option)
- World-class operation (option)
  - Call progress, blacklisting, multiple country support
- Communication software compatible AT command sets
- NVRAM directory and stored profiles
- Built-in DTE interfaces with speed up to 115.2 kbps
  - Parallel 16550A UART-compatible interface
  - Serial ITU-T V.24 (EIA/TIA-232-E)
- Supports Rockwell PnP ISA Bus Interface Device
- Supports Serial PnP interface per Plug and Play External COM Device Specification, Rev 1.00
- Serial async data; parallel async data
- Caller ID and distinctive ring detect
- Single package: 68-pin PLCC
- +5V operation

1.3 TECHNICAL OVERVIEW

1.3.1 General Description

The single device provides the processing core for a complete system design featuring data/fax modem, AudioSpan, speakerphone, audio, voice, and VoiceView support depending on model (Table 1-1). The OEM adds a crystal, discrete components, and a telephone line/telephone/audio interface circuit to complete the system.

The modem is packaged in a 68-pin PLCC.

The modem is the full-featured, self-contained data modem/fax modem/voice/audio/speakerphone solution shown in Figure 1-1 (serial DTE interface) and Figure 1-2 (parallel host interface). Dialing, call progress, telephone line interface, AudioSpan, speakerphone, voice/audio, and VoiceView functions are supported and controlled through the AT command set.

The modem connects to the DTE via a V.24 (EIA/TIA-232-E) serial interface or to a host via a parallel microcomputer bus depending on modem model.

1.3.2 Data/Fax Modes

In data modem modes, the modem can operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33600 bps (RCV336) or 14400 bps (RCV144). Data modem modes perform complete handshake and data rate negotiations. All tone and pattern detection functions required by the applicable ITU or Bell standard are supported. For RCV336, using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps to 300 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330.

In fax modem modes, the modem fully supports Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, or 2400 bps. Fax modem modes support Group 3 fax requirements. Fax data transmission and reception performed by the modem is controlled and monitored through the fax EIA-578 Class 1 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking is provided.

Both transmit and receive fax data are buffered within the modem. Data transfer to and from the DTE is flow controlled by XON/XOFF and RTS/CTS.

1.3.3 AudioSpan Modes

AudioSpan provides full-duplex analog simultaneous audio/voice and data over a single telephone line. AudioSpan can send any type of audio waveform, including music. Data can be sent with or without error correction. The audio/voice interface can be in the form of a headset, handset, or a microphone and speaker (half-duplex speakerphone).

V.61 Modulation. AudioSpan can operate in V.61 modulation at a data rate with audio of 4800 bps.

ML144 Modulation. AudioSpan can operate in ML144 (V.32) modulation at a 4.8 to 9.6 kbps data rate with audio where lower data rates provide higher audio quality.

ML288 Modulation (RCV336/RC336 Only). AudioSpan can operate in ML288 (V.34 type) modulation at a 4.8 to 14.4 kbps data rate with audio where lower data rates provide higher audio quality.

1.3.4 Speakerphone Mode (SP Models Only)

The speakerphone mode features an advanced proprietary speakerphone algorithm which supports full-duplex voice conversation with both acoustic and line echo cancellation. Parameters are constantly adjusted to maintain stability with automatic fallback from full-duplex to pseudo-duplex operation. The speakerphone algorithm allows position independent placement of microphone and speaker.

The speakerphone mode provides hands-free full-duplex telephone operation under host control. The host can separately control microphone gain and muting and speaker volume and muting.

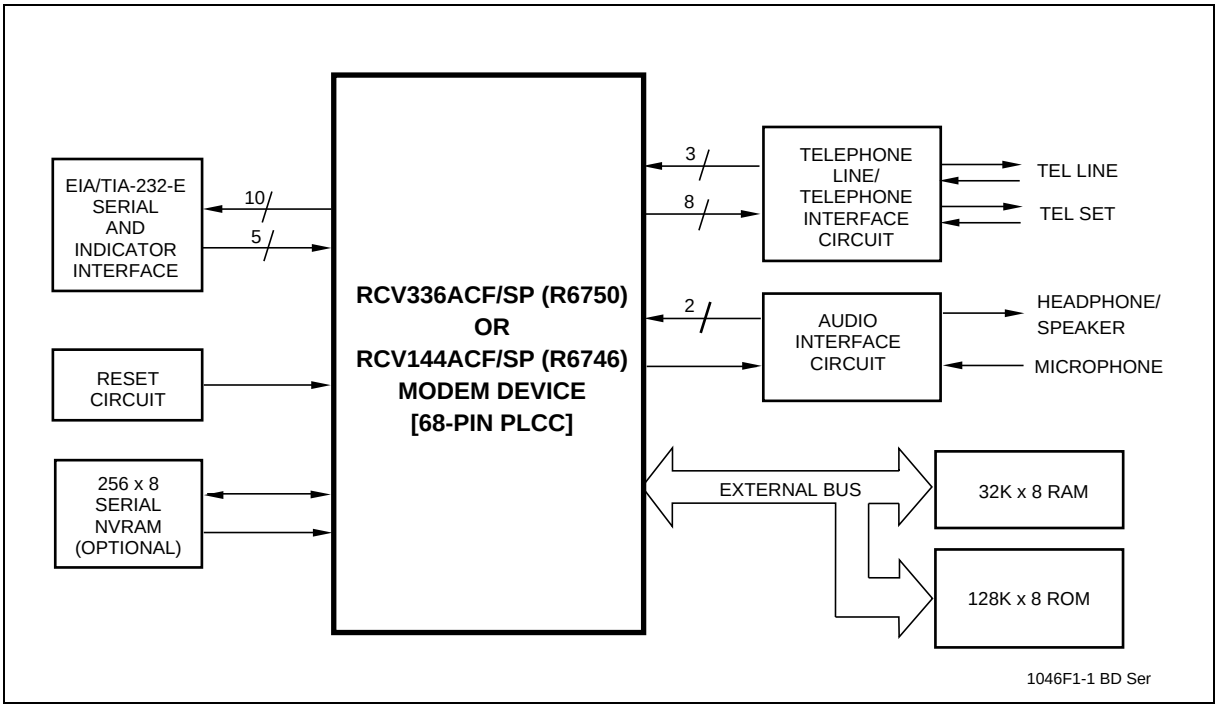

Figure 1-1. Block Diagram - Serial DTE Interface

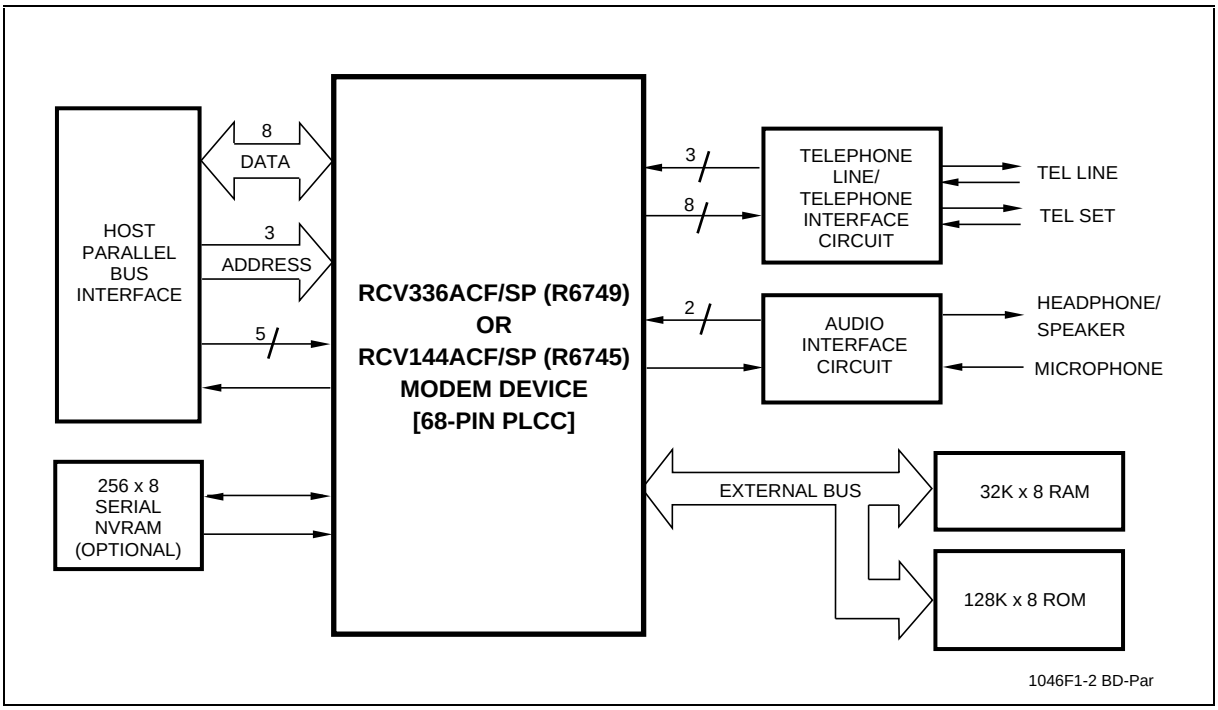

Figure 1-2. Block Diagram - Parallel Host Interface

1.3.5 Modem Firmware

Modem firmware performs processing of general modem control, command sets, fax Class 1, AudioSpan, speakerphone, data modem, fax modem, voice/audio/TAM/speakerphone, VoiceView, W-class, and DTE/host interface functions.

Configurations of the modem firmware are provided to support parallel host bus interface operation or serial DTE interface operation.

The modem firmware is provided in object code form for the OEM to program into external ROM. The modem firmware may also be provided in source code form under a source code addendum license agreement.

1.3.6 Supported Interfaces

The major hardware signal interfaces of the modem device are illustrated in Figure 1-1 (serial DTE interface) and Figure 1-2 (parallel host interface).

Parallel Host Bus Interface

A 16550A UART-compatible parallel host bus interface is supported. The interface signals are: eight bidirectional data lines (HD0-HD7), three address input lines (HA0-HA2), three control input lines (~HCS, ~HRD, and ~HWT), one status output line (HINT), and a reset input line (-RESET).

Serial DTE Interface and Indicator Outputs

A V.24/EIA/TIA-232-E logic-compatible DTE serial interface is provided in the serial interface version. One serial transmit data input line (~TXD), one serial receive data output line (~RXD), four control input lines (~DTR, ~RTS, ~RDL, and ~AL), and six status output lines (~CTS, ~DSR, ~RLSD, ~TM, ~RI, and ~DRSOUT) are supported.

Three dedicated indicator output lines (~DTRIND, ~TMIND, and ~AAIND) are also provided.

NVRAM Interface

A two-line serial interface to an optional OEM-supplied non-volatile RAM (NVRAM) is provided. The interface signals are a bidirectional data line (NVMDATA) and a clock output line (NVMCLK). Data stored in NVRAM can take precedence over the factory default settings. A 256-byte NVRAM can store up to two user-selectable configurations and can store up to four 35-digit dial strings.

External RAM and ROM Interface

The modem external bus connects to OEM-supplied 128-kbyte ROM and 32-kbyte RAM. This non-multiplexed external bus supports eight bidirectional data lines (D0-D7), 17 address output lines (A0-A16), two read/write control output lines (~READ and ~WRITE), and two chip select output lines (~ROMSEL and ~RAMSEL).

External ROM and RAM access time must be 45 ns or faster.

Telephone Line/Telephone/Audio Interface

The Telephone Line/Telephone/Audio Signal Interface can support either a 2-relay telephone line interface without Caller ID relay (Figure 1-3) or a 3-relay telephone line interface using a Caller ID relay (Figure 1-4). In either case, the Caller ID function is supported.

Receive/Transmit Data. A receive analog input (RIN) and a transmit analog output (TXA1) are supported.

Relay Controls. Relay control outputs to the line interface are supported:

- Off-hook (~RLY1)
- Caller ID (~CALLID) (The 2 relay design shown in Figure 1-3 supports the Caller ID function without using the ~CALLID relay control output.)
- Voice (~VOICE)
- Mute (~MUTE) (Enabled by ConfigurACE II.)

Signal routing for Voice mode is shown in Table 1-2.

Relay positions for VoiceView are shown in Table 1-3.

Ring Detect. A ring detect (RINGD) input is supported.

Loop Current Sense. A loop current sense (LCS) input is supported.

Microphone Input and Speakerphone Output. Two microphone inputs are supported: one for voice input (MICV) and one for sound input (MICM), e.g., music-on-hold.

The MICV and SPKV lines connect to the handset and speaker to support functions such as AudioSpan headset and speakerphone modes, FDSP, telephone emulation, microphone voice record, speaker voice playback, and call progress monitor.

The MICM input can accept an external audio signal to support the music-on-hold function (selected by the #VLS=7 command) and routes it to the telephone line. In this case, the modem can be configured using ConfigurACE II to either bandlimit the signal to satisfy FCC part 68 requirements or allow DTMF detection during the music-on-hold function. If music-on-hold function is not required, the microphone signal can be connected to the MICM input to support telephone emulation mode (selected by the #VLS=5 command).

The speaker output (SPKV) carries the normal speakerphone audio or reflects the received analog signals in the modem.

Telephone Input and Telephone Output. An input from the telephone microphone (TELIN) and an output to the telephone speaker (TELOUT) are supported in AudioSpan modes. These lines connect voice record/playback and AudioSpan audio to the local handset.

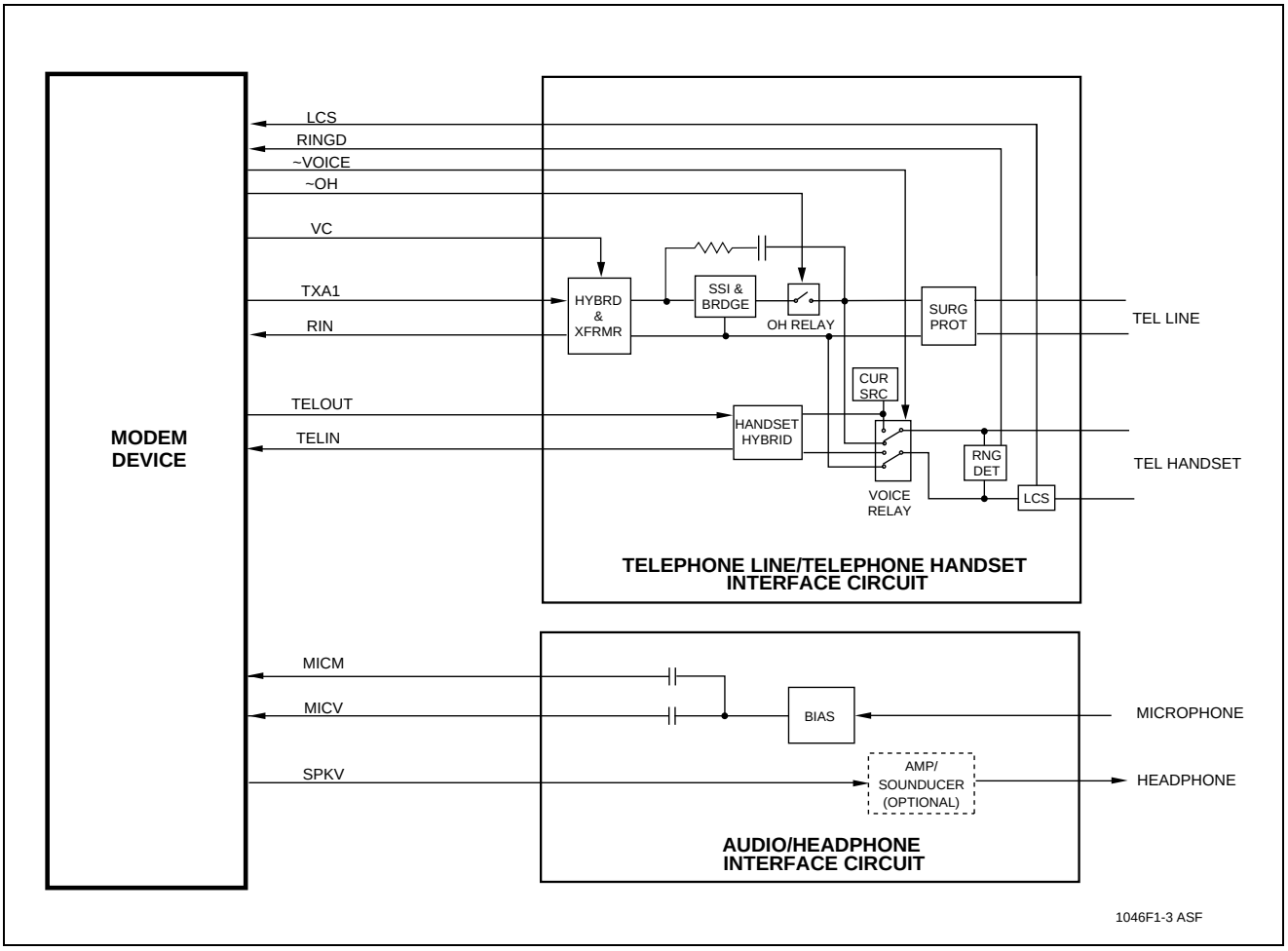

Figure 1-3. 2-Relay Telephone Line/ Telephone/Audio Signal Interface (U.S.)

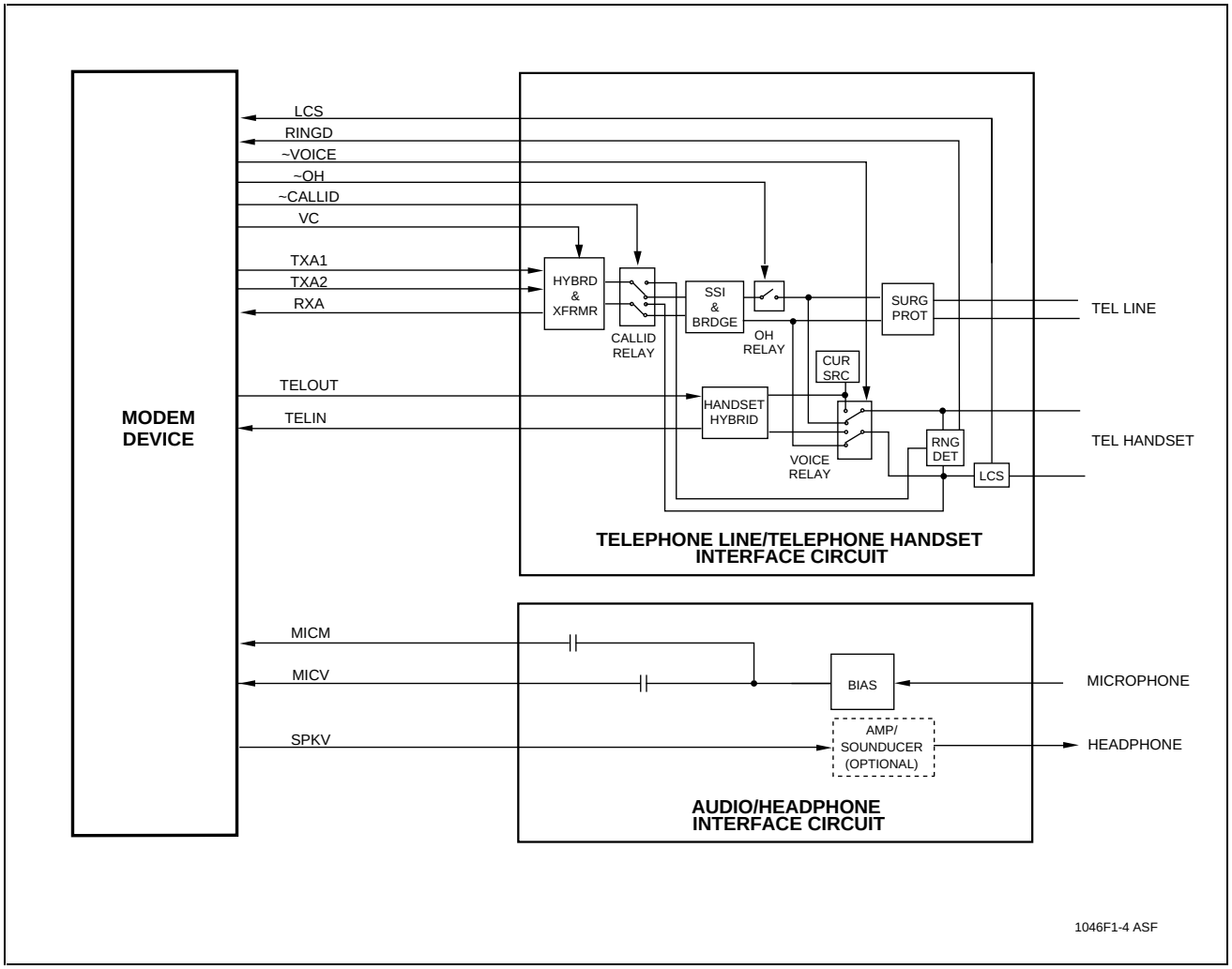

Figure 1-4. 3-Relay Telephone Line/ Telephone/Audio Signal Interface (U.S.)

Table 1-2. Signal Routing - Voice Mode (#CLS=8)

2-Relay DAA					
#VLS=	**Mode Function**	**Input Selected**	**Output Selected**	**Off-Hook Relay (~OH) Activated**	**Voice Relay (~VOICE) Activated**
0	Modem with modem speaker output disabled	RXA	TXA	Yes	No
1	Record from or playback to handset	TELIN	TELOUT	No	Yes
2	Playback to modem speaker	RXA	TXA and SPKV	No	No
3	Microphone input for local recording	MICV	TXA	No	Yes
4	Modem with modem speaker output enabled	RXA	TXA and SPKV	Yes	No
5	Reserved				
6	Use speakerphone after dialing or answering	RXA and MICV	TXA and SPKV	Yes	No
7	Mute local handset; sound chips output to telephone line (music on hold)	MICM	TXA and SPKV	No[1]	Yes
8	Record conversation through sound chips	RXA	SPKV	No[1]	No
9	Record/playback from local handset through sound chips	TELIN and MICV	TELOUT and SPKV	No	Yes

3-Relay DAA						
#VLS=	**Mode Function**	**Input Selected**	**Output Selected**	**Caller ID Relay (~CALLID) Activated**	**Off-Hook Relay (~OH) Activated**	**Voice Relay (~VOICE) Activated**
0	Modem with modem speaker output disabled	RXA	TXA	No	Yes	No
1	Record from or playback to handset	TELIN	TELOUT	Yes	No	Yes
2	Playback to modem speaker	RXA	TXA and SPKV	Yes	No	No
3	Microphone input for local recording	MICV	TXA	Yes	No	Yes
4	Modem with modem speaker output enabled	RXA	TXA and SPKV	No	Yes	No
5	Reserved					
6	Use speakerphone after dialing or answering	RXA and MICV	TXA and SPKV	No	Yes	No
7	Mute local handset; sound chips output to telephone line (music on hold)	MICM	TXA and SPKV	No	No[1]	Yes
8	Record conversation through sound chips	RXA	SPKV	Yes	No[1]	No
9	Record/playback from local handset through sound chips	RXA and MICM	TELOUT and SPKV	Yes	No	Yes

NOTES:

1. The offhook relay should be previously activated, e.g., by an ATA or ATD command.
2. SPKV = SPKV output enabled.

Table 1-3. Relay Positions - VoiceView Mode (+FCLASS=80)

2-Relay DAA			
Stage	**Function**	**Off-Hook Relay (~OH) Activated**	**Voice Relay (~VOICE) Activated**
1	On-hook	No	No
2a	Detected tone - on-hook	No	No
2b	Detected tone - off-hook for handset and speakerphone	Yes	No
3	Off-hook	Yes	Yes

3-Relay DAA				
Stage	**Function**	**Caller ID Relay (~CALLID) Activated**	**Off-Hook Relay (~OH) Activated**	**Voice Relay (~VOICE) Activated**
1	On-hook	No	No	No
2a	Detected tone - on-hook	Yes	No	No
2b	Detected tone - off-hook for handset and speakerphone	Yes	Yes	No
3	Off-hook	No	Yes	Yes

1.3.7 Commands

The modem supports data modem, fax class 1 modem, voice/audio, full-duplex speakerphone (FDSP), MNP 10/MNP 10EC, and VoiceView commands, and S Registers in accordance with modem model options (see Section 7).

Data Modem Operation. Data modem functions operate in response to the AT commands when +FCLASS=0. Default parameters support US/Canada operation.

MNP 10 Operation. MNP 10 functions operate in response to MNP 10 commands.

MNP 10EC Operation. MNP 10EC is enabled by the -SEC=1 command.

AutoSync Operation. AutoSync operates in response to the &Q4 command.

Fax Modem Operation. Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or #CLS=1.

Voice Operation. Voice mode functions operate in response to voice/audio commands when #CLS=8, #VSR=7200 [default], and either #VBS=2 or #VBS=4 is selected.

Audio Operation. Audio mode functions operate in response to voice/audio commands when #CLS=8, #VSR=7200 [default] or #VSR=11025, and #VBS=8 is selected.

Speakerphone Operation. FDSP functions operate in response to speakerphone commands when #CLS=8 and #VLS=6 is selected.

World Class (W-Class) Operation. Models supporting W-class functions operate in response to W-class AT commands.

VoiceView Operation. VoiceView functions operate in response to VoiceView commands when +FCLASS=80.

1.3.8 ConfigurACE II for Windows Utility Program

The PC-based ConfigurACE II for Windows utility program allows the OEM to customize the modem firmware to suit specific application and country requirements. ConfigurACE II for Windows allows programming of functions such as:

- Loading of multiple sets of country parameters
- Loading of NVRAM factory profiles
- Call progress and blacklisting parameters
- Entry of S register maximum/minimum values
- Limitation of transmit levels
- Modification of factory default values
- Customization of the ATI4 response
- Customization of fax OEM messages

This program modifies the hex object code which can be programmed directly into the system EPROM. Lists of the generated parameters can be displayed or printed.

Rockwell-provided country parameter files allow a complete set of country-specific call progress and blacklisting parameters to be selected.

Refer to the ConfigurACE II for Windows software for a detailed description of capabilities and the operating procedure.

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2. TECHNICAL SPECIFICATIONS

2.1 SERIAL DTE INTERFACE OPERATION

2.1.1 Automatic Speed/Format Sensing

Command Mode and Data Modem Mode. The modem can automatically determine the speed and format of the data sent from the DTE. The modem can sense speeds of 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 19200, 38400, and 57600 bps (RC144), or 300, 600, 1200, 2400, 4800, 7200, 9600, 12000, 14400, 16800, 19200, 21600, 24000, 26400, 28800, 38400, 57600, and 115200 bps (RC336), and the following data formats:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Character Length (No. of Bits)
None	7	2	10
Odd	7	1	10
Even	7	1	10
None	8	1	10
Odd	8	1	11*
Even	8	1	11*

* 11-bit characters are sensed, but the parity bits are stripped off during data transmission in Normal and Error Correction modes.

The modem can speed sense data with mark or space parity and configures itself as follows:

DTE Configuration	Modem Configuration
7 mark	7 none
7 space	8 none
8 mark	8 none
8 space	8 even

Fax Modem Mode. The DTE to modem data rate is 19200 bps.

2.2 PARALLEL HOST BUS INTERFACE OPERATION

Command Mode and Data Modem Mode. The modem can operate at rates up to 57600 bps (RC144) or 115200 (RC336) by programming the Divisor Latch in the parallel interface registers.

Fax Modem Mode. The host to modem data rate is 19200 bps.

2.3 ESTABLISHING DATA MODEM CONNECTIONS

Telephone Number Directory

The modem supports four telephone number entries in a directory that can be saved in a serial NVRAM. Each telephone number can be up to 35 characters in length. A telephone number can be saved using the &Zn=x command, and a saved telephone number can be dialed using the DS=n command.

Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with ITU-T Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

Call Progress Tone Detection

Ringback, equipment busy, and progress tones can be detected in accordance with the applicable standard.

Answer Tone Detection

Answer tone can be detected over the frequency range of 2100 ± 40 Hz in ITU-T modes and 2225 ± 40 Hz in Bell modes.

Ring Detection

A ring signal can be detected from a TTL-compatible 15.3 Hz to 68 Hz square wave input.

Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for 2 seconds (data modem) or 4 seconds (fax adaptive answer) to allow transmission of the billing signal.

Connection Speeds

The modem functions as a data modem when the +FCLASS=0 or #CLS=0 command is active.

Line connection can be selected using the +MS command in accordance with the draft PN-3320 standard presented to the TR30-4 committee (which is a candidate for the definition of V.25 ter at the ITU). The +MS command selects modulation, enables/disables automode, and selects minimum and maximum line speeds (Table 2-1).

ATNn and S37=n commands are supported up to V.32 bis speeds (Table 2-2).

For RC144, the F command is also supported (Table 2-2).

Automode

Automode detection can be enabled by the +MS command to allow the modem to connect to a remote modem in accordance with draft PN-3320 for V.34 (Table 2-1).

Alternatively, N1 commands allow the modem to connect to a remote modem in accordance with EIA/TIA-PN2330 for V.32 bis speeds and lower (Table 2-2).

2.4 DATA MODE

Data mode exists when a telephone line connection has been established between modems and all handshaking has been completed.

Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send data to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

Flow Control

DTE-to-Modem Flow Control. If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

Escape Sequence Detection

The "+++" escape sequence can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by an S2 Register value greater than 127.

BREAK Detection

The modem can detect a BREAK signal from either the DTE or the remote modem. The \Kn command determines the modem response to a received BREAK signal.

Telephone Line Monitoring

GSTN Cleardown (V.34, V.32 bis, V.32). Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Loss of Carrier (V.22 bis and Below). If carrier is lost for a time greater than specified by the S10 register, the modem disconnects (except MNP 10).

Receive Space Disconnect (V.22 bis and Below). If selected by the Y1 command in non-error-correction mode, the modem disconnects after receiving 1.6 ± 10% seconds of continuous SPACE.

Table 2-1. +MS Command Automode Connectivity

<mod>	Modulation	Possible Rates (bps) [1]	Notes
0	V.21	300	
1	V.22	1200	
2	V.22 bis	2400 or 1200	
3	V.23	1200	See Note 2
9	V.32	9600 or 4800	
10	V.32 bis	14400, 12000, 9600, 7200, or 4800	Default
11	V.34	33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, or 4800	RCV336ACF family
64	Bell 103	300	
69	Bell 212	1200	

Notes:

1. See optional <automode>, <min_rate>, and <max_rate> subparameters for the +MS command.
2. For V.23, originating modes transmit at 75 bps and receive at 1200 bps; answering modes transmit at 1200 bps and receive at 75 bps. The rate is always specified as 1200 bps.
3. If the DTE speed is set to less than the maximum supported DCE speed in automode, the maximum connection speed is limited to the DTE speed.

Table 2-2. Command Connections

ATF Setting[1,2]	ATN Setting[1,2]	S37 Setting	ATB Setting	Speed Sensed	Connection
Note 3	0	0	0	300	V.21
Note 3	0	0	0	1200	V.22 1200
Note 3	0	0	X	2400	V.22 bis 2400
Note 3	0	0	X	4800	V.32 bis/V.32 4800
Note 3	0	0	X	7200	V.32 bis 7200
Note 3	0	0	X	9600	V.32 bis/V.32 9600
Note 3	0	0	X	12000	V.32 bis 12000
Note 3	0	0	X	Higher	V.32 bis 14400
Note 3	0	0	1	300	Bell 103
Note 3	0	0	1	1200	Bell 212A
ATF1	0	1-3	0	X	V.21
ATF4	0	5	0	X	V.22 1200
ATF5	0	6	X	X	V.22 bis 2400
ATF1	0	1-3	1	X	Bell 103
ATF4	0	5	1	X	Bell 212A
ATF3	0	7	X	X	V.23
ATF6	0	8	X	X	V.32 bis/V.32 4800
ATF8	0	9	X	X	V.32 bis/V.32 9600
ATF7	0	12	X	X	V.32 bis 7200
ATF9	0	10	X	X	V.32 bis 12000
ATF10	0	11	X	X	V.32 bis 14400
ATF0	1	X	X	X	Automode

Notes:

1. ATFn can be used in lieu of ATN0 and S37. ATFn (where n = valid number) sets ATN0 and S37 to the corresponding value.
2. ATF0 forces ATN1 and S37=0.
3. The connection speed is determined by DTE speed sensing (serial interface only). A subsequent ATFn command supersedes the ATN and S37 settings.

Send SPACE on Disconnect (V.22 bis and Below)

If selected by the Y1 command in non-error-correction mode, the modem sends 4 ± 10% seconds of continuous SPACE when a locally commanded hang-up is issued by the &Dn or H command.

2.4.2 Fall Forward/Fallback (V.34/V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within V.34/V.32 bis/V.32 mode depending upon signal quality if automode is enabled by the +MS or N1 command.

When connected in V.34/V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the current modulation depending upon signal quality if fall forward/fallback is enabled by the %E2 command.

Retrain

The modem may lose synchronization with the received line signal under poor line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved, or until 30 seconds elapse resulting in line disconnect.

Programmable Inactivity Timer

The modem disconnects from the line if data is not sent or received for a specified length of time. In normal or error-correction mode, this inactivity timer is reset when data is received from either the DTE or from the line. This timer can be set to a value between 0 and 2550 seconds by using register S30. A value of 0 disables the inactivity timer.

DTE Signal Monitoring (Serial DTE Interface Only)

~DTR. When ~DTR is asserted, the modem responds in accordance with the &Dn and &Qn commands.

~RTS. ~RTS is used for flow control if enabled by the &K command in normal or error-correction mode.

~RDL. When ~RDL is asserted, the modem requests a remote digital loop if connected in non-error-correction mode.

~AL. When ~AL is asserted, the modem disconnects and enters analog loop.

2.5 ERROR CORRECTION AND DATA COMPRESSION

V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a fallback, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the best method of error correction between two modems.

MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. Supporting stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

V.42 bis Data Compression

V.42 bis data compression mode, enabled by the %Cn command or S46 register, operates when a LAPM or MNP 10 connection is established.

The V.42 bis data compression employs a "string learning" algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two 2k-byte dictionaries are used to store the strings. These dictionaries are dynamically updated during normal operation.

MNP 5 Data Compression

MNP 5 data compression mode, enabled by the %Cn command, operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

2.6 MNP 10 DATA THROUGHPUT ENHANCEMENT

MNP 10 protocol and MNP Extended Services enhance performance under adverse channel conditions such as those found in rural, long distance, or cellular environments. An MNP 10 connection is established when an MNP 2-4 connection is negotiated with a remote modem supporting MNP 10.

MNP Extended Services. The modem can quickly switch to MNP 10 operation when the remote modem supports MNP 10 and both modems are configured to operate in V.42.

V.42 bis/MNP 5 Support. V.42 bis/MNP 10 can operate with V.42 bis or MNP 5 data compression.

2.7 MNP 10EC™ ENHANCED CELLULAR CONNECTION

A traditional landline modem, when used for high-speed cellular data transmission, typically encounters frequent signal interference and degradation in the connection due to the characteristics of the analog cellular network. In this case, cellular-specific network impairments, such as non-linear distortion, fading, hand-offs, and high signal-to-noise ratio, contribute to an unreliable connection and lower data transfer performance. Implementations relying solely on protocol layer methods, such as MNP 10, generally cannot compensate for the landline modem's degraded cellular channel performance.

The modem achieves higher cellular performance by implementing enhanced cellular connection techniques at both the physical and protocol layers, depending on modem model. The modem enhances the physical layer within the modulation by optimizing its responses to sudden changes in the cellular connection. The MNP 10EC protocol layer implemented in the modem firmware improves data error identification/correction and maximizes data throughput by dynamically adjusting speed and packet size based on signal quality and data error performance.

2.8 AUTOSYNC

Hayes AutoSync mode, when used with communications software incorporating the Hayes Synchronous Interface (HSI), provides synchronous communication capabilities from an asynchronous data terminal. In AutoSync, the modem places the call asynchronously then automatically switches to synchronous operation once the telephone connection has been established. AutoSync allows communication from an asynchronous DTE (typically a personal computer) to synchronous DTE (typically a mainframe computer or minicomputer).

2.9 FAX CLASS 1 OPERATION

Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or #CLS=1.

In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by fax commands. Some AT commands are still valid but may operate differently than in data modem mode.

Calling tone is generated in accordance with T.30.

2.10 VOICE/AUDIO MODE

Voice and audio functions are supported by the Voice Mode. Voice Mode includes three submodes: Online Voice Command Mode, Voice Receive Mode, and Voice Transmit Mode.

2.10.1 Online Voice Command Mode

This mode results from the connection to the telephone line or a voice/audio I/O device (e.g., microphone, speaker, or handset) through the use of the #CLS=8 and #VLS commands. After mode entry, AT commands can be entered without aborting the connection.

2.10.2 Voice Receive Mode

This mode is entered when the #VRX command is active in order to record voice or audio data input at the RXA pin, typically from a microphone/handset or the telephone line.

Received analog voice samples are converted to digital form and compressed for reading by the host. AT commands control the codec bits-per-sample rate.

Received analog mono audio samples are converted to digital form and formatted into 8-bit unsigned linear PCM format for reading by the host. AT commands control the bit length and sampling rate. Concurrent DTMF/tone detection is available at the 7200 Hz sample rate.

2.10.3 Voice Transmit Mode

This mode is entered when the #VTX command is active in order to playback voice or audio data to the TXA1 output, typically to a speaker/handset or to the telephone line.

Digitized voice data is decompressed and converted to analog form at the original compression quantization sample-per-bits rate then output to the TXA1 output.

Digitized audio data is converted to analog form then output to the TXA1 output.

2.10.4 Audio Mode

The audio mode enables the host to transmit and receive 8-bit audio signals. In this mode, the modem directly accesses the internal analog-to-digital (A/D) converter (ADC) and the digital-to-analog (D/A) converter (DAC). Incoming analog audio signals can then be converted to digital format and digital signals can be converted to analog audio output.

2.10.5 Tone Detectors

The tone detector signal path is separate from the main received signal path thus enabling tone detection to be independent of the configuration status. In Tone Mode, all three tone detectors are operational.

2.10.6 Speakerphone Modes

Speakerphone modes are selected in voice mode with the following #VLS= commands:

Use Speakerphone After Dialing or Answering (#VLS=6). #VLS=6 selects speakerphone mode while in #CLS=8 mode. Speakerphone operation is entered during Voice Online Command mode after completing dialing or answering.

Speakerphone Settings (#SPK = Parameters). The #SPK command can be used to control the microphone state (mute or on), adjust the speaker volume, and microphone gain. The #SPK parameters are valid only after the modem has entered the Voice Online mode while in the #VLS=6 setting. The command syntax is:

#SPK=<mute>,<spkr>,<mic> (See the AT Command Reference Manual for exact syntax.)

<mute> = Mute Mode Select (Range = 0-2)
- 0 = microphone mute
- 1 = microphone on (default)
- 2 = Room Monitor mode (microphone gain is maximum and speaker output is off)

<spkr> = Speaker Output Level Attenuation
- Range = 0 to 15 (in 2 dB steps)
- Default = 10 (20 dB)
- Speaker mute = 16

<mic>= Microphone Gain Value (Range = 0-3)
- 0 = 0 dB gain
- 1 = 10 dB gain
- 2 = 15 dB gain (default)
- 3 = 20 dB gain

Room Monitor Feature. The Room Monitor function allows an application where a remote caller calls the computer to monitor sound in a room. For example, the #SPK=2,,, command selects a listen only mode where the microphone gain is set to maximum and the speaker output is off.

2.10.7 Sound Card Support Modes

Sound card support modes are selected in voice mode with the following #VLS= commands:

Mute Handset; Route Sound Chips Output To Line (#VLS=7). #VLS=7 mutes the local handset and routes the sound chip output (such as music or messages during telephone hold) by switching the handset out of the telephone line path if in #VLS=0 or #VLS=4 mode (valid after the modem is offhook, e.g., from an ATA or ATD command).

Record Conversation through Sound Chips (#VLS=8). #VLS=8 engages the Caller ID relay to allow recording of conversation through sound chips (valid after the modem is offhook, e.g., from an ATA or ATD command).

Recording/Playback from Local Handset through Sound Chips (#VLS=9). #VLS=9 routes the handset lines to the sound chips to allow recording/playback of audio through the local handset.

2.11 SIMULTANEOUS AUDIO/VOICE AND DATA (AUDIOSPAN)

The modem can operate in AudioSpan Mode if the remote modem is also configured for AudioSpan Mode operation.

AT commands are used to select the AudioSpan Mode (-SMS command), to enable automatic AudioSpan modulation selection or select a specific AudioSpan modulation (-SQS command), and to enable AudioSpan data burst operation (-SMC command).

ML288 Modulation. ML288 (V.34 type) modulation supports 4.8 to 14.4 kbps data speeds with audio where the lower data rates provide higher audio quality. The ML288 data speed with audio is six data speeds below the capability supported by telephone line quality (up to 28800 bps). For example, a connection that can support V.34 28800 bps data speed will cause a resulting AudioSpan ML288 data-only speed to be 28800 bps and the data speed with audio to be 14400 bps. A ML288 data speed with audio will upshift to its corresponding higher data-only speed when the handset is placed on-hook.

ML144 Modulation. ML144 (V.32 bis) modulation supports 4.8 to 9.6 kbps data speeds with audio where the lower data rates provide higher audio quality. The ML144 data speed plus audio is at least two data speeds below the capability supported by telephone line quality. For example, a connection that can support V.32 bis 14400 bps data speed will cause a resulting AudioSpan data speed with audio to be between V.61/4800 and ML144/9600. A ML144 data speed with audio will upshift to higher data-only speed when no audio/voice is detected.

V.61 Modulation. V.61 modulation supports 4800 bps data speed with audio, and a data-only speed of 4800 bps.

2.11.1 Supported Data Speeds

Table 2-3 lists the data speed when the handset is on-hook (ML288) or audio is not present (ML144), and the data speed when audio is present, based upon the selected AudioSpan modulation.

Table 2-3. AudioSpan Data Speeds

AudioSpan Modulation	Data Speed (bps) [When the Handset is On-hook (ML288) or Audio is Not Present (ML144)]	Data Speed (bps) with Audio [When Audio is Present]
ML288	28800 (Note 2)	14400 (Note 2)
ML288	26400	12000 (Note 2)
ML288	24000	9600 (Note 2)
ML288	21600	7200 (Note 2)
ML288	19200 to 4800	4800 (Note 2)
ML144	14400	9600, 7200, or 4800
ML144	12000	7200 or 4800
ML144	9600 to 4800	4800
V.61	4800	4800

Notes:

1. Applicable when the handset is on-hook (#VLS=0) or during headset operation (AT#VLS=5) or speakerphone operation (#VLS=6).
2. 28800 bps is the highest ML288 data-only speed supported.

2.11.2 AudioSpan Mode Selection

AudioSpan Mode is selected with the -SMS=2 (AudioSpan Mode) or the -SMS=3 (Automatic DSVD/AudioSpan/Data Only Mode Select) command. The local modem should be set to the AudioSpan Mode (-SMS=2) when sending, and to the AudioSpan Mode (-SMS=2) or Automatic DSVD/AudioSpan/Data Only Mode Select (-SMS=3) when receiving. The -SMS command definition is:

-SMS = x, y, z, t (Select AudioSpan/DSVD/Data Mode)

The x parameter selects Data, AudioSpan, or DSVD Mode, or enables automatic mode selection. The y, z, and t parameters are optional and are required only if the user wishes to control connection speeds. For example, AT-SMS=2 selects AudioSpan Mode.

x: Data/AudioSpan/DSVD mode select and automatic mode select enable

0 =	Data Mode	(Default) (data-only mode, AudioSpan and DSVD are disabled)
1 =	DSVD mode	(Note: AT-SMS=1 performs the same operation at AT-SSE=1)
2 =	AudioSpan mode	
3 =	Automatic mode select	(Data/DSVD/AudioSpan)

y: Minimum data speed (bps) with audio for AudioSpan Mode (see y value in following table)

z: Maximum data speed (bps) with audio for AudioSpan Mode (see z value in following table)

	Modulation Selected (See -SQS Command)		
y or z Value	**V.61**	**ML144**	**ML288**
4800	S (y and z Default)	S (y Default)	S (y Default)
7200	—	S	S
9600	—	S (z Default)	S
12000	—	—	S
14400	—	—	S (z Default)

S = Supported.
— = Not supported.

t: Symbol rate (ML288 modulation only)

0 =	Auto Selection	(Default)
1 - 6 =	Reserved	

Examples

1. AT -SMS=2 selects AudioSpan Mode (the y, z, and t parameters are not required).
2. AT -SMS=2,4800,9600 selects AudioSpan Mode, specifies the minimum data speed with audio of 4800 bps, and specifies the maximum data speed with audio of 9600 bps.

2.11.3 AudioSpan Modulation Select and Enable/Disable AudioSpan Automatic Modulation Selection

The host can enable the modem to select the optimal modulation or select a specific modulation. The -SQS command definition is:

-SQS = x, y (Select AudioSpan Modulation and Enable/Disable AudioSpan Automatic Modulation Selection)

x: Select AudioSpan modulation

0 =	V.61	
1 =	ML144	(Default for RCV144)
2 =	ML288	(Default for RCV336)

y: Enable/disable AudioSpan automatic modulation (automodulation) selection

0 =	Disable AudioSpan automodulation	(Host selects AudioSpan modulation specified by the x parameter. If the selected modulation is not supported by the modem, ERROR is reported and the x parameter is not changed. If the remote modem does not support the selected modulation, the modem disconnects.)
1 =	Enable AudioSpan automodulation	(Default. The modem starts with the AudioSpan modulation specified by the x parameter and falls back from ML288, to ML144, to V.61, or to data mode (e.g., V.34 or V.32 bis) depending on the selected x parameter, the remote modem capability, and line conditions.)

The AT-SQS parameters should remain at default unless a particular modulation is preferred.

Examples

1. AT -SQS=2,1 enables AudioSpan automodulation starting with ML288 modulation.
2. AT -SQS=2,0 disables AudioSpan automodulation and selects ML288 modulation.
3. AT -SQS=1,0 disables AudioSpan automodulation and selects ML144 modulation.

2.11.4 ML144 Data Burst Option

ML144 data burst can be enabled using the -SMC command in ML144 modulation. Data burst will keep the audio channel open only when energy is detected on the handset or headset. When silence is detected in data burst mode, the connected modems will upshift in speed for higher throughput. Disabling data burst mode will keep the audio channel open at all times during the AudioSpan connection. The -SMC command definition is:

-SMC = x (Enable/Disable ML144 Data Burst)

0 =	Disable data burst	
1 =	Enable data burst	(Default)

2.11.5 AudioSpan Audio Interface

The AudioSpan audio interface defaults to the local handset connected to the modem (AT#VLS=0) and can be configured to interface through the modem microphone and speaker pins to support use of a headset (AT#VLS=5) or a speakerphone (AT#VLS=6).

2.11.6 Audio Quality Considerations.

AudioSpan audio quality is dependent upon modulation mode, data rate and telephone line quality. Some guidelines are:

1. Higher quality telephone lines provide better audio quality than impaired telephone lines.
2. A lower data speed with audio provides better audio quality than higher data speed with audio. For example, a ML288/9600 connection will be audibly superior to a ML288/14400 connection.

3. For identical data speed with audio using different modulations (e.g., ML144 vs. ML288), the audio quality at ML288 will be superior. For example, a ML288/9600 will be audibly superior to a ML144/9600 connection.

2.12 FULL-DUPLEX SPEAKERPHONE (FDSP) MODE

The modem operates in FDSP mode when #CLS=8 and #VLS=6 (see 2.10.6).

In FDSP Mode, speech from a microphone or handset is converted to digital form, shaped, and output to the telephone line through the line interface circuit. Speech received from the telephone line is shaped, converted to analog form, and output to the speaker or handset. Shaping includes both acoustic and line echo cancellation.

2.13 VOICEVIEW

Voice and data can be alternately sent and received in a time-multiplexed fashion over the telephone line whenever the +FCLASS=80 command is active. This command and other VoiceView commands embedded in host communications software control modem operation. Most VoiceView commands use an extended syntax starting with the characters "-S", which signifies the capability to switch between voice and data.

2.14 CALLER ID

Caller ID can be enabled/disabled using the #CID command. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem.

2.15 WORLD CLASS COUNTRY SUPPORT

The W-class models include functions which support modem operation in multiple countries. The following capabilities are provided in addition to the data modem functions previously described. Country dependent parameters are all programmable by ConfigurACE II for Windows.

2.15.1 Dialing

Dial Tone Detection. Dial tone detection levels and frequency ranges are programmable by ConfigurACE II for Windows.

DTMF Dialing. Transmit output level, DTMF signal duration, and DTMF interdigit interval parameters are programmable by ConfigurACE II for Windows.

Pulse Dialing. Parameters such as make/break times, set/clear times, and dial codes are programmable by ConfigurACE II for Windows.

Ring Detection. The frequency range is programmable by ConfigurACE II for Windows.

Blind Dialing. Blind dialing may be disabled by ConfigurACE II for Windows.

2.15.2 Carrier Transmit Level

The carrier transmit level can be programmed through S91 for data and S92 for fax. The maximum, minimum, and default values can be defined by ConfigurACE II for Windows to match specific country and DAA requirements.

2.15.3 Calling Tone

Calling tone is generated in accordance with V.25. Calling tone may be toggled (enabled/disabled) by inclusion of a "^" character in a dial string. It may also be disabled by programming a country specific parameter using ConfigurACE II for Windows.

2.15.4 Call Progress Tone Detection

Frequency and cadence of tones for busy, ringback, congested, dial tone 1, and dial tone 2 are programmable by ConfigurACE II for Windows.

2.15.5 Answer Tone Detection

The answer tone detection period is programmable by ConfigurACE II for Windows.

2.15.6 Blacklist Parameters

The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted"). Up to 40 such numbers may be tabulated. The blacklist parameters are established by ConfigurACE II for Windows.

2.15.7 Relay Control

On-hook/off-hook, make/break, and set/clear relay control parameters are programmable by ConfigurACE II for Windows.

The NVMDATA line can additionally be assigned as the ~MUTE relay control by ConfigurACE II for Windows.

2.16 DIAGNOSTICS

2.16.1 Commanded Tests

Diagnostics are performed in response to &T commands.

Analog Loopback (&T1 Command). Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

Analog Loopback with Self Test (&T8 Command). An internally generated test pattern of alternating 1s and 0s (reversals) is sent to the modem. An error detector within the modem checks for errors in the string of reversals.

Remote Digital Loopback (RDL) (&T6 Command). Data from the local DTE is sent to the remote modem which loops the data back to the local DTE.

Remote Digital Loopback with Self Test (&T7 Command). An internally generated pattern is sent from the local modem to the remote modem, which loops the data back to the local modem.

Local Digital Loopback (&T3 Command). When local digital loop is requested by the local DTE, two data paths are set up in the local modem. Data from the local DTE is looped back to the local DTE (path 1) and data received from the remote modem is looped back to the remote modem (path 2).

2.16.2 Power On Reset Tests

Upon power on, the modem performs tests of the modem, internal RAM, ROM, and NVRAM. If the modem, internal RAM, or ROM test fails, the ~TMIND output is pulsed (serial interface version) or the DCD bit in the parallel interface register is pulsed (parallel interface version) as follows:

Internal RAM test fails: One pulse cycle (pulse cycle = 0.5 sec. on, 0.5 sec. off) every 1.5 seconds.

ROM test fails: Two pulse cycles every 1.5 seconds.

Modem device test fails: Three pulse cycles every 1.5 seconds.

If the NVRAM test fails (due to NVRAM failure or if NVRAM is not installed), the test failure is reported by AT commands that normally use the NVRAM, e.g., the &V command.

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3. HARDWARE INTERFACE

3.1 HARDWARE SIGNALS

The modem hardware interface signals for the serial DTE interface configuration are shown in Figure 3-1.

The modem hardware interface signals for the parallel host interface configuration are shown in Figure 3-2.

The modem pin assignments for the 68-pin PLCC with serial DTE interface are shown in Figure 3-3 and are listed in Table 3-1.

The modem pin assignments for the 68-pin PLCC with parallel host interface are shown in Figure 3-4 and are listed in Table 3-2.

The modem hardware interface signals are defined in Table 3-3.

The digital electrical characteristics for the hardware interface signals are listed in Table 3-4.

The analog electrical characteristics for the hardware interface signals are listed in Table 3-5.

The current and power requirements are listed in Table 3-6.

The absolute maximum ratings are listed in Table 3-7.

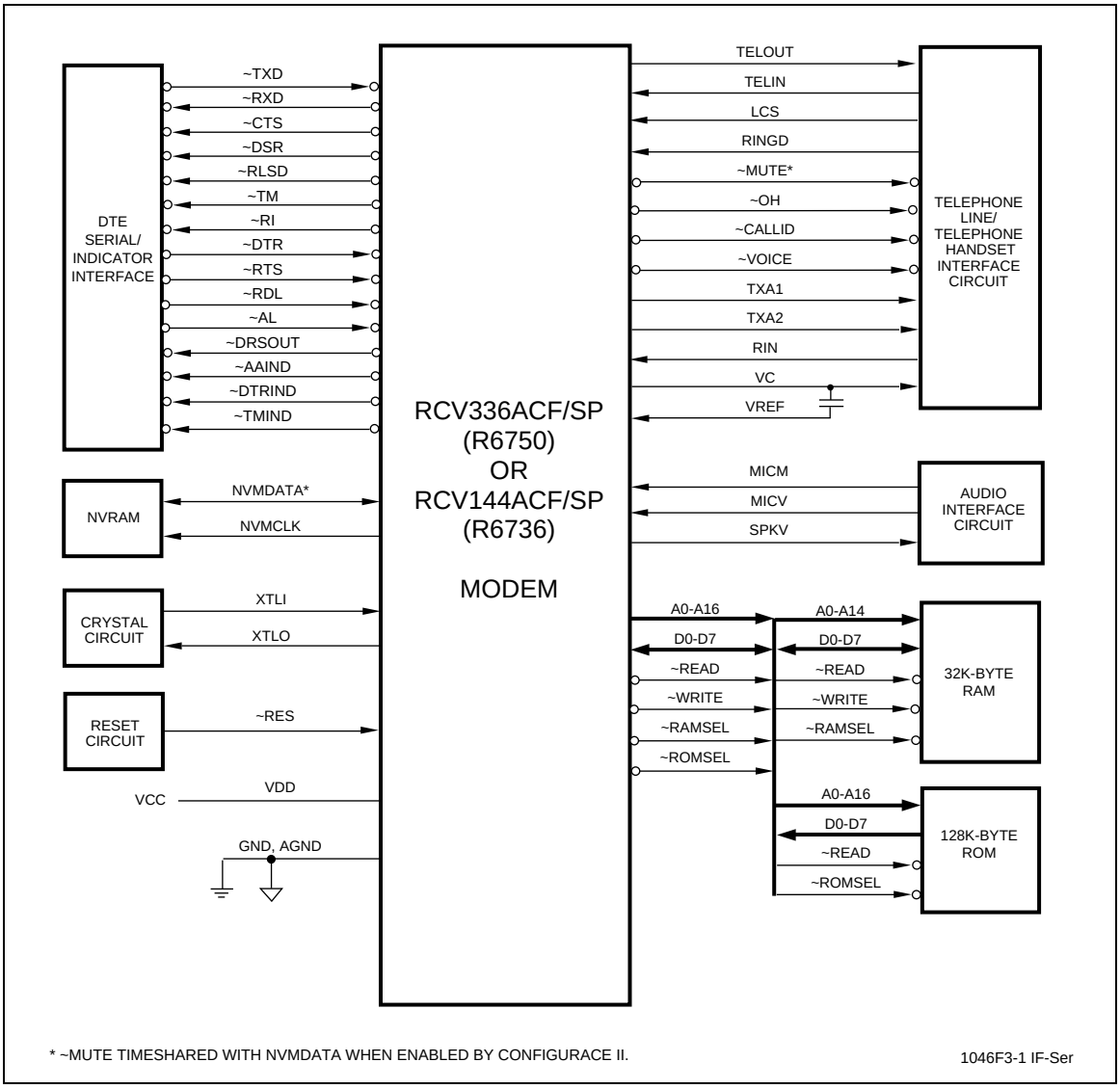


Figure 3-1. Hardware Interface Signals - Serial DTE Interface

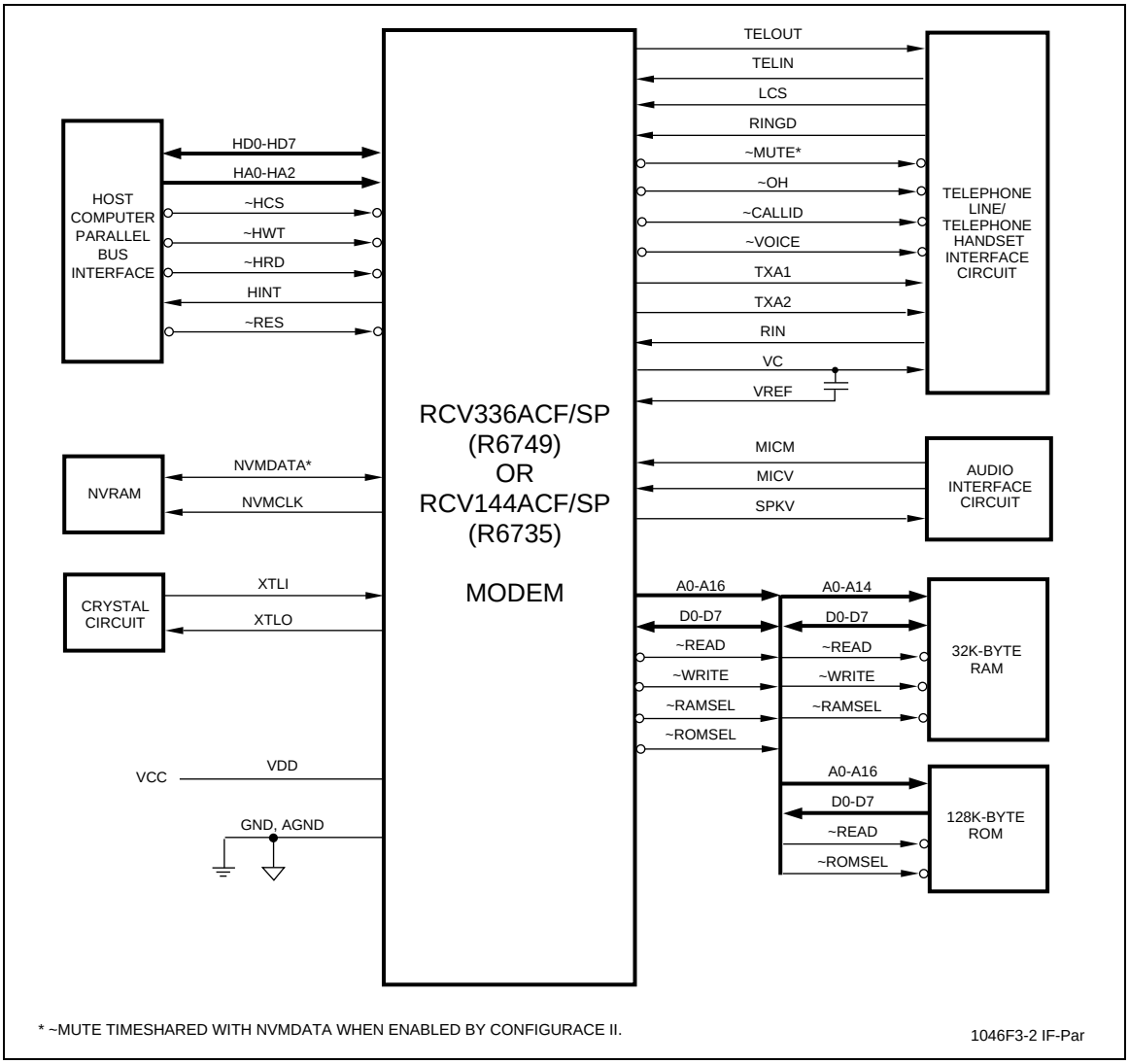


Figure 3-2. Hardware Interface Signals - Parallel Host Interface

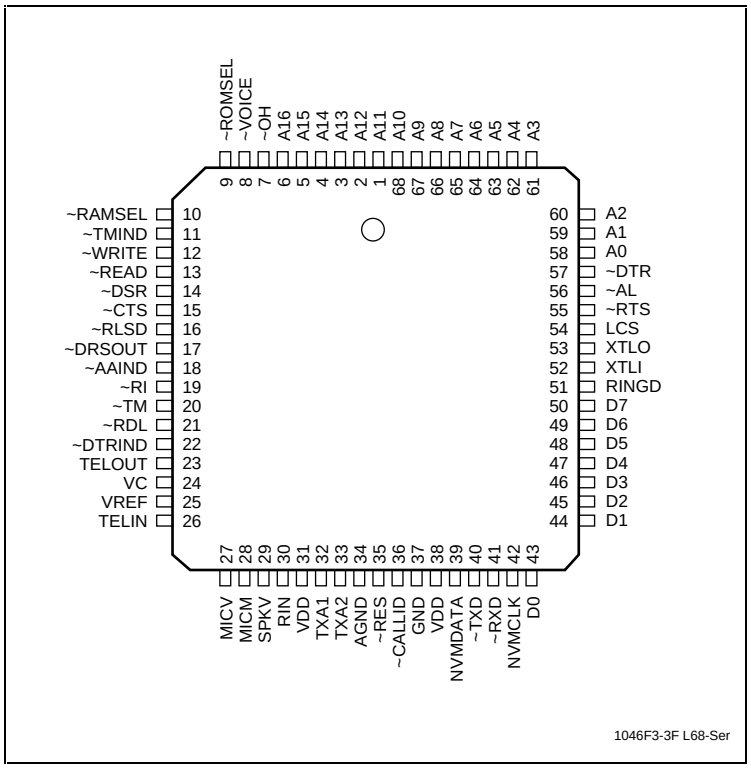


Figure 3-3. Modem Pin Signals - 68-Pin PLCC - Serial DTE Interface

Table 3-1. Modem Pin Signals - 68-Pin PLCC - Serial DTE Interface

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	A11	OA	EB: A11	35	~RES	IC	HB: (Note 4)
2	A12	OA	EB: A12	36	~CALLID	OA	DAA: ~CALLID
3	A13	OA	EB: A13	37	GND	GND	GND
4	A14	OA	EB: A14	38	VDD	PWR	VCC and filter
5	A15	OA	EB: A15	39	NVMDATA/ ~MUTE	IA/OA OA	NVRAM: SDA (Note 3)/ DAA: ~MUTE (Note 5)
6	A16	OA	EB: A16	40	~TXD	IA	DTE: ~TXD
7	~OH	OA	DAA: ~OH	41	~RXD	OA	DTE: ~RXD
8	~VOICE	OA	DAA: ~VOICE	42	NVMCLK	OA	NVRAM: SCL
9	~ROMSEL	OA	ROM: ~CE	43	D0	IA/OA	EB: D0
10	~RAMSEL	OA	RAM: ~CS	44	D1	IA/OA	EB: D1
11	~TMIND	OA	Indicator Circuit	45	D2	IA/OA	EB: D2
12	~WRITE	OA	EB: ~WRITE	46	D3	IA/OA	EB: D3
13	~READ	OA	EB: ~READ	47	D4	IA/OA	EB: D4
14	~DSR	OB	DTE: ~DSR	48	D5	IA/OA	EB: D5
15	~CTS	OB	DTE: ~CTS	49	D6	IA/OA	EB: D6
16	~RLSD	OB	DTE: ~RLSD	50	D7	IA/OA	EB: D7
17	~DRSOUT	OB	DTE: ~DRSOUT	51	RINGD	IA	DAA: RINGD
18	~AAIND	OA	Indicator Circuit	52	XTLI	IE	XTLI
19	~RI	OB	DTE: ~RI	53	XTLO	OE	XTLO
20	~TM	OB	DTE: ~TM	54	LCS	IA	DAA: LCS
21	~RDL	IA	DTE: ~RDL	55	~RTS	IA	DTE: ~RTS
22	~DTRIND	OA	Indicator Circuit	56	~AL	IA	DTE: ~AL
23	TELOUT	O(DD)	Telephone Handset Interface	57	~DTR	IA	DTE: ~DTR
24	VC	DI	AGND through capacitors and DAA	58	A0	OA	EB: A0
25	VREF	DI	VC through capacitors	59	A1	OA	EB: A1
26	TELIN	I(DA)	Telephone Handset Interface	60	A2	OA	EB: A2
27	MICV	I(DA)	Audio Interface	61	A3	OA	EB: A3
28	MICM	I(DA)	Audio Interface	62	A4	OA	EB: A4
29	SPKV	O(DD)	Audio Interface	63	A5	OA	EB: A5
30	RIN	I(DA)	DAA: RXA	64	A6	OA	EB: A6
31	VDD	PWR	VCC and filter	65	A7	OA	EB: A7
32	TXA1	O(DD)	DAA: TXA1	66	A8	OA	EB: A8
33	TXA2	O(DD)	DAA: TXA2	67	A9	OA	EB: A9
34	AGND	GND	AGND	68	A10	OA	EB: A10

Notes:

1. I/O types:
   - DI = Device interconnect.
   - IA, IC = Digital input; IE = Crystal input (see Table 3-4).
   - OA, OB, = Digital output; OE = Crystal output (see Table 3-4).
   - I(DA) = Analog input (see Table 3-5).
   - O(DD), O(DF) = Analog output (see Table 3-5).
2. NC = No external connection allowed.
3. Connect to VCC through 10K ohms.
4. Connect to GND through 10K ohms.
5. ~MUTE use can be enabled by ConfigurACE II for Windows.

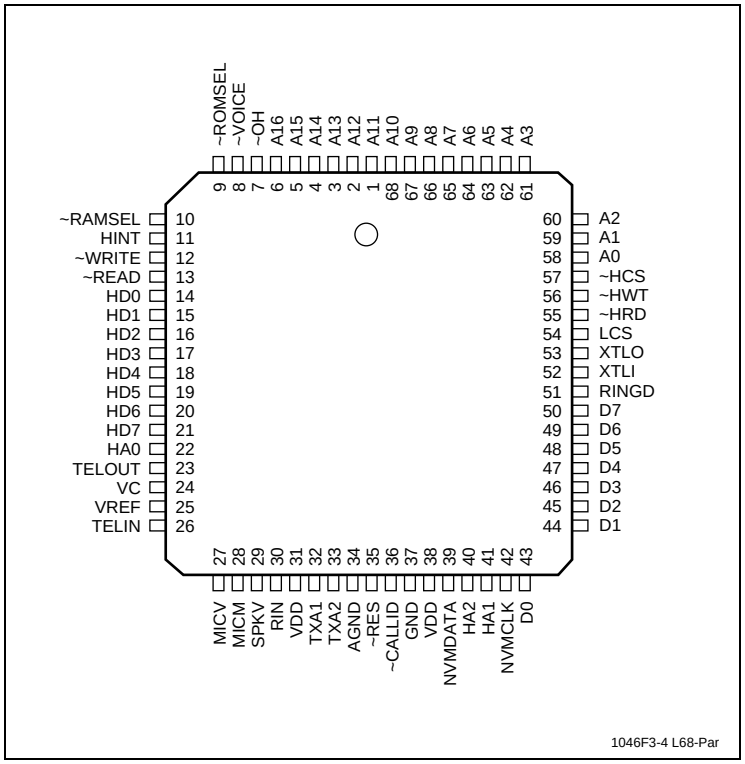


Figure 3-4. Modem Pin Signals- 68-Pin PLCC - Parallel Host Interface

Table 3-2. Modem Pin Signals- 68-Pin PLCC - Parallel Host Interface

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	A11	OA	EB: A11	35	~RES	IC	HB: (Note 4)
2	A12	OA	EB: A12	36	~CALLID	OA	DAA: ~CALLID
3	A13	OA	EB: A13	37	GND	GND	GND
4	A14	OA	EB: A14	38	VDD	PWR	VCC and filter
5	A15	OA	EB: A15	39	NVMDATA/ ~MUTE	IA/OA OA	NVRAM: SDA (Note 3)/ DAA: ~MUTE (Note 5)
6	A16	OA	EB: A16	40	HA2	IA	HB: HA2
7	OH	OA	DAA: ~OH	41	HA1	IA	HB: HA1
8	~VOICE	OA	DAA: ~VOICE	42	NVMCLK	OA	NVRAM: SCL
9	~ROMSEL	OA	ROM: ~CE	43	D0	IA/OA	EB: D0
10	~RAMSEL	OA	RAM: ~CS	44	D1	IA/OA	EB: D1
11	HINT	OA	HB: HINT	45	D2	IA/OA	EB: D2
12	~WRITE	OA	EB: ~WRITE	46	D3	IA/OA	EB: D3
13	~READ	OA	EB: ~READ	47	D4	IA/OA	EB: D4
14	HD0	IA/OB	HB: HD0	48	D5	IA/OA	EB: D5
15	HD1	IA/OB	HB: HD1	49	D6	IA/OA	EB: D6
16	HD2	IA/OB	HB: HD2	50	D7	IA/OA	EB: D7
17	HD3	IA/OB	HB: HD3	51	RINGD	IA	DAA: RINGD
18	HD4	IA/OB	HB: HD4	52	XTLI	IE	XTLI
19	HD5	IA/OB	HB: HD5	53	XTLO	OE	XTLO
20	HD6	IA/OB	HB: HD6	54	LCS	IA	DAA: LCS
21	HD7	IA/OB	HB: HD7	55	~HRD	IA	HB: ~RD
22	HA0	IA	HB: HA0	56	~HWT	IA	HB: ~WT
23	TELOUT	O(DD)	Telephone Handset Interface	57	~HCS	IA	HB: ~CS
24	VC	DI	AGND through capacitors and DAA	58	A0	OA	EB: A0
25	VREF	DI	VC through capacitors	59	A1	OA	EB: A1
26	TELIN	I(DA)	Telephone Handset Interface	60	A2	OA	EB: A2
27	MICV	I(DA)	Audio Interface	61	A3	OA	EB: A3
28	MICM	I(DA)	Audio Interface	62	A4	OA	EB: A4
29	SPKV	O(DD)	Audio Interface	63	A5	OA	EB: A5
30	RIN	I(DA)	DAA: RXA	64	A6	OA	EB: A6
31	VDD	PWR	VCC and filter	65	A7	OA	EB: A7
32	TXA1	O(DD)	DAA: TXA1	66	A8	OA	EB: A8
33	TXA2	O(DD)	DAA: TXA2	67	A9	OA	EB: A9
34	AGND	GND	AGND	68	A10	OA	EB: A10

Notes:

1. I/O types:
   - DI = Device interconnect.
   - IA, IC = Digital input; IE = Crystal input (see Table 3-4).
   - OA, OB, = Digital output; OE = Crystal output (see Table 3-4).
   - I(DA) = Analog input (see Table 3-5).
   - O(DD), O(DF) = Analog output (see Table 3-5).
2. NC = No external connection allowed.
3. Connect to VCC through 10K ohms.
4. Connect to GND through 10K ohms.
5. ~MUTE use can be enabled by ConfigurACE II for Windows.

Table 3-3. Modem Pin Signal Definitions

Label	I/O Type	Signal Name/Description
		GENERAL
XTLI, XTLO	IE, OE	**Modem Crystal/Clock In and Crystal Out.** Connect to an external crystal circuit consisting of a crystal and passive components. The crystal frequency is 52.416 MHz.
~RES	IC	**Modem Reset.** The active low ~RES input resets the modem logic, and restores the saved configuration from NVRAM or returns the modem to the factory default values if NVRAM is not present. ~RES low holds the modem in the reset state; ~RES going high releases the modem from the reset state. After application of +5V, ~RES must be held low for at least 15 ms after the +5V power reaches operating range. The modem device set is ready to use 25 ms after the low-to-high transition of ~RES. For serial Interface, the ~RES input is typically connected to a reset switch circuit. For parallel Interface, the ~RES input is typically connected to the host bus RESET line through an inverter.
VDD	PWR	**+ 5V Supply Voltage.** Connect to VCC.
GND	GND	**Digital Ground.** Connect to digital ground.
AGND	GND	**Analog Ground.** Connect to analog ground.
		NVRAM INTERFACE
NVMCLK	OA	**NVRAM Clock.** NVMCLK output high enables the NVRAM.
NVMDATA	IA/OA	**NVRAM Data.** The NVMDATA pin supplies a serial data interface to the NVRAM. This line can also be timeshared with ~PULSE output as enabled by ConfigurACE II for Windows.
		EXTERNAL MEMORY BUS INTERFACE
A0-A16	OA	**Address Lines 0-16.** A0-A16 are the external memory bus address output lines.
D0-D7	IA/OA	**Data Line 0-7.** D0-D7 are the external memory bus bidirectional data lines.
~READ	OA	**Read Enable.** ~READ output low enables data transfer from the selected device to the D0-D7 lines.
~WRITE	OA	**Write Enable.** ~WRITE output low enables data transfer from the D0-D7 lines to the selected device.
~RAMSEL	OA	**RAM Select.** ~RAMSEL output low selects the external RAM.
~ROMSEL	OA	**ROM Select**. ~ROMSEL output low selects an external ROM or flash ROM.
		TELEPHONE LINE INTERFACE
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 ½ load.
RIN	I(DA)	**Receive Analog.** RIN is a single-ended receive data input from the telephone line/audio interface.
~OH	OA	**Off-Hook Relay Control.** The active low ~OH output is used to control the normally open off-hook relay. The ~PULSE function is also provided on this line for single ~OH/~PULSE relay application.
LCS	IA	**Loop Current Sense.** LCS is an active high input that indicates a handset off-hook status.
RINGD	IA	**Ring Frequency.** A rising edge on the RINGD input initiates an internal ring frequency measurement. The RINGD input is typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low.
VC	MI	**Centerpoint Voltage.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) capacitors in parallel and a ferrite bead in series with the capacitors (see Section 5).
VREF	MI	**Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.

Table 3-3. Modem Pin Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
~VOICE	OD	**Voice Relay Control.** The ~VOICE output is connected to the Voice relay (DPDT). In voice mode, the modem asserts the this output to switch the handset from the telephone line to a current source to power the handset so it can be used as a microphone and speaker interface to the modem. This relay output is used in conjunction with the ~CALLID and ~OH relay outputs to configure the telephone line/telephone/audio interface circuit (see Table 1-2). The ~VOICE output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor, such as an MPSA20, can be used to drive heavier loads (e.g., electro-mechanical relays).
~CALLID	OD	**Caller ID Relay Control.** For a 3-relay DAA design, the ~CALLID output is connected to the Caller ID relay (DPDT). When Caller ID is enabled, the modem closes the Off-hook relay and asserts this output to switch the Caller ID in order to detect Caller ID information between the first and second rings. This relay output is used in conjunction with the ~VOICE and ~OH relay outputs to configure the telephone line/telephone/audio interface circuit (see Table 3a). The ~CALLID output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor, such as an MPSA20, can be used to drive heavier loads (e.g., electro-mechanical relays).
~MUTE	OA	**Mute Relay Control.** When enabled by ConfigurACE II for Windows, the NVMDATA line can be assigned to the ~MUTE output. In this case, the active low ~MUTE output can be used to control the normally open mute relay.
TELEPHONE HANDSET INTERFACE		
TELIN	I(DA)	**Telephone Handset Input.** TELIN is the input from the telephone handset microphone interface circuit.
TELOUT	O(DF)	**Telephone Handset Output.** TELOUT is the output to the telephone handset speaker interface circuit.
AUDIO/HEADSET INTERFACE		
MICM	I(DA)	**Microphone Modem Input.** MICM is a single-ended microphone input from the analog switch circuit. The input impedance is > 70k ohms.
MICV	I(DA)	**Microphone Voice Input.** MICV is a single-ended microphone input from the analog switch circuit. The input impedance is > 70k ohms.
SPKV	O(DF)	**Speaker Output.** Speakerphone speaker out is a single ended output.
PARALLEL HOST INTERFACE (PARALLEL INTERFACE VERSION) The parallel interface emulates a 16550A UART-compatible interface.		
HA0-HA2	IA	**Host Bus Address Lines 0-2.** During a host read or write operation with ~HCS low, HA0-HA2 select an internal 16550A-compatible register.
HD0-HD7	IA/OB	**Host Bus Data Lines 0-7**. HD0-HD7 are comprised of eight three-state input/output lines providing bidirectional communication between the host and the modem. Data, control words, and status information are transferred over HD0-HD7.
~HCS	IA	**Host Bus Chip Select. ~**HCS input low enables the modem host bus interface.
~HRD	IA	**Host Bus Read.** ~HRD is an active low, read control input. When ~HCS is low, ~HRD low allows the host to read status information or data from a selected modem register.
~HWT	IA	**Host Bus Write.** ~HWT is an active low, write control input. When ~HCS is low, ~HWT low allows the host to write data or control words into a selected modem register.
HINT	OA	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt is asserted. HINT is reset low upon the appropriate interrupt service or master reset operation.

Table 3-3. Modem Pin Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
V.24 (EIA/TIA-232-E) DTE SERIAL INTERFACE AND INDICATOR (SERIAL INTERFACE VERSION)		
The serial interface signals correspond to logically inverted V.24 / EIA/TIA-232-E signals with TTL voltage levels.		
~TXD	IA	**Transmitted Data (EIA BA/ITU-T CT103).** The DTE uses the ~TXD line to send data to the modem for transmission over the telephone line or to transmit commands to the modem.
~RXD	OA	**Received Data (EIA BB/ITU-T CT 104).** The modem uses the ~RXD line to send data received from the telephone line to the DTE and to send modem responses to the DTE. During command mode, ~RXD data represents the modem responses to the DTE.
~CTS	OB	**Clear To Send (EIA CB/ITU-T CT106).** ~CTS output ON (low) indicates that the modem is ready to accept data from the DTE. In asynchronous operation, in error correction or normal mode, ~CTS is always ON (low) unless RTS/CTS flow control is selected by the &Kn command.
~DSR	OB	**Data Set Ready (EIA CC/ITU-T CT107).** ~DSR indicates modem status to the DTE. ~DSR OFF (high) indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (~RI). ~DSR output is controlled by the AT&Sn command.
~RLSD	OB	**Received Line Signal Detector (EIA CF/ITU-T CT109).** When AT&C0 command is not in effect, ~RLSD output is ON when a carrier is detected on the telephone line or OFF when carrier is not detected.
~TM	OB	**Test Mode Indicate (EIA TM/ITU-T CT142).** The ~TM output indicates the modem is in test mode (low) or in any other mode (high).
~RI	OB	**Ring Indicator (EIA CE/ITU-T CT125).** ~RI output ON (low) indicates the presence of an ON segment of a ring signal on the telephone line.
~DRSOUT	OB	**Data Signaling Rate Indicator (EIA CI/ITU-T CT112).** ~DRSOUT is ON (low) when the modem desires or is engaged in the high speed (2400 bps or higher) mode. ~DRSOUT is OFF (high) otherwise.
~DTR	IA	**Data Terminal Ready (EIA CD/ITU-T CT108).** The ~DTR input is turned ON (low) by the DTE when the DTE is ready to transmit or receive data. ~DTR ON prepares the modem to be connected to the telephone line, and maintains the connection established by the DTE (manual answering) or internally (automatic answering). ~DTR OFF places the modem in the disconnect state under control of the &Dn and &Qn commands.
~RTS	IA	**Request To Send (EIA CA/ITU-T CT105).** ~RTS input ON (low) indicates that the DTE is ready to accept data from the modem. In the command state, the modem ignores ~RTS. In asynchronous operation, the modem ignores ~RTS unless RTS/CTS flow control is selected by the &Kn command.
~RDL	IA	**Remote Digital Loop Select (EIA RL/ITU-T CT140).** ~RDL input low activates remote digital loop request. The loop is executed at the speed for which the modem is currently configured.
~AL	IA	**Analog Loop (EIA LL/ITU-T CT141).** ~AL input low causes the modem to operate in the analog loop test mode.
~AAIND	OA	**Auto Answer Indicator.** ~AAIND output ON (low) corresponds to the indicator on. ~AAIND output is active when the modem is configured to answer the ring automatically (ATSO command ≠0).
~TMIND	OA	**Test Mode Indicator.** ~TMIND output ON (low) corresponds to the indicator on. ~TMIND output pulses (indicator flashes) when the modem is in test mode and if an error is detected.
~DTRIND	OA	**DTR Indicator.** ~DTRIND output ON (low) corresponds to the indicator on. The ~DTRIND state reflects the ~DTR output state except when the &D0 command is active, in which case ~DTRIND is low.

Notes:

1. I/O types:
   - DI = Device interconnect.
   - IA, IC = Digital input; IE = Crystal input (see Table 3-4).
   - OA, OB, = Digital output; OE = Crystal output (see Table 3-4).
   - I(DA) = Analog input (see Table 3-5).
   - O(DD), O(DF) = Analog output (see Table 3-5).
2. NC = No external connection allowed.

Table 3-4. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				VDC	
Type IA and IB		2.0	–	VCC + 0.3		
Type IC and ID		0.7 V_{CC}	–	VCC + 0.3		
Type IE		–	4.0	–		Note 2.
Input High Current	I_{IH}				µA	VCC = 5.25 V, V_{IN}= 5.25 V
Type IB		–	–	40		
Type IC		–	–	2.5		
Input Low Voltage	V_{IL}				VDC	
Type IA, IB, ID		–0.3	–	0.8		
Type IC		–0.3	–	0.8		
Type IE		–	1.0	–		Note 2.
Input Low Current	I_{IL}				µA	VCC = 5.25 V
Type IB and IC		–	–	-400		
Input Leakage Current	I_{IN}				µADC	
Types IA and ID		15	–	100		V_{IN} = 0 to 0 V
XTLI		–	–	±10		V_{IN} = 0 to V_{CC}
Output High Voltage	V_{OH}				VDC	
Type OA		2.4	–	–		I_{LOAD} = – 100 µA
Type OB		2.4	–	–		I_{LOAD} = – 6 mA
Type OD		–	–	V_{CC}		I_{LOAD} = 0 mA
Type OE						Note 3.
Output Low Voltage	V_{OL}				VDC	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 6 mA
Type OD		–	–	0.75		I_{LOAD} = 15 mA
Three-State (Off) Current	I_{TSI}			±10	µADC	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}			±10	µADC	V_{IN} = 0.4 to VCC-1
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA and ID			–	10		
Type IB			–	20		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC			–	10		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type IC						CMOS with pull-up
Type ID						~RES
Types OA and OB						TTL with 3-state
Type OC						Open drain
Type OD						Relay driver

Notes:

1. Test Conditions: VCC = ±5%, TA = 0°C to 70°C, (unless otherwise stated).
   Output loads: Data bus (D0-D7), address bus (A0-A15), chip selects, ~READ, and ~WRITE loads = 70 pF + one TTL load.
   Other = 50 pF + one TTL load.
2. Type IE inputs are centered approximately 2.5 V and swing 1.5 V_{PEAK} in each direction.
3. Type OE outputs provide oscillator feedback when operating with an external crystal.

Table 3-5. Analog Electrical Characteristics

Name	Type	Characteristic	Value
RIN,	I (DA)	Input Impedance	> 70K Ω
TELIN		AC Input Voltage Range	1.1 VP-P**
		Reference Voltage	+2.5 VDC
TXA1,	O (DD)	Minimum Load	300 Ω
TXA2,		Maximum Capacitive Load	0 µF
TELOUT		Output Impedance	10 Ω
		AC Output Voltage Range	2.2 VP-P
		Reference Voltage	+2.5 VDC
		DC Offset Voltage	± 200 mV
SPKV	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	1.1 VP-P
		Reference Voltage	+2.5 VDC
		DC Offset Voltage	± 20 mV
MICM,	I (DA)	Input Impedance	> 70K Ω
MICV		Maximum AC Input Voltage	1.7 VP-P
		Reference Voltage*	+2.5 VDC
		Maximum AC Output Voltage	2.7 VP-P

* Reference Voltage provided internal to the device.

** Corresponds to 2.2 VP-P at Tip and Ring.

Table 3-6. Current and Power Requirements

Mode	Current (ID)		Power (PD)		Notes
	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)	
Normal mode	170	205	850	1075	

Notes:
Test conditions: VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.

Table 3-7. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA

3.2 INTERFACE TIMING AND WAVEFORMS

3.2.1 External Memory Bus Timing

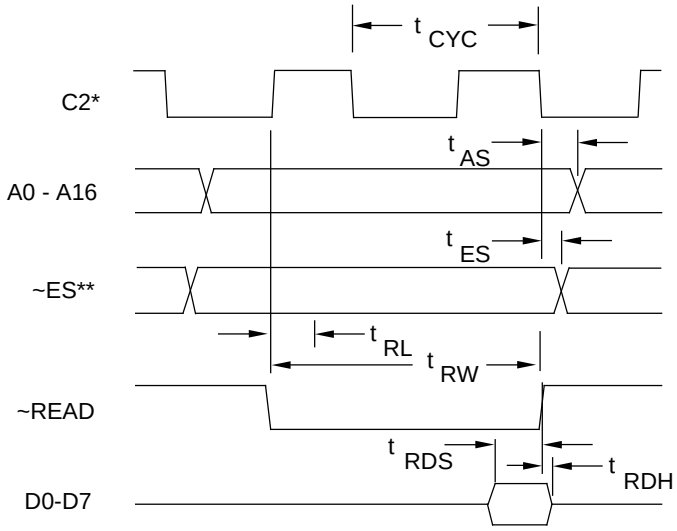
The external memory bus timing is listed in Table 3-8 and illustrated in Figure 3-5.

Table 3-8. Timing - External Memory Bus

Symbol	Parameter	Min	Typ.	Max	Units
t_{CYC}	Internal Operating Cycle	38.16			ns
Read					
t_{AS}	~READ High to Address Valid	–	17	20	ns
t_{ES}	~READ High to ES Valid	–	18	21	ns
t_{RW}	~READ Pulse Width	57.2		–	ns
t_{RDS}	Read Data Valid to ~READ High	8.7		–	ns
t_{RDH}	~READ High to Read Data Hold	0		–	ns
Write					
t_{AS}	~WRITE High to Address Valid	–	16	19.5	ns
t_{ES}	~WRITE High to ES Valid	–	18	21	ns
t_{WW}	~WRITE to ~WRITE Pulse Width	57.2		–	ns
t_{WTD}	~WRITE Low to Write Data Valid	–	13	15	ns
t_{WTH}	~WRITE High to Write Data Hold	5.0		–	ns

Notes:

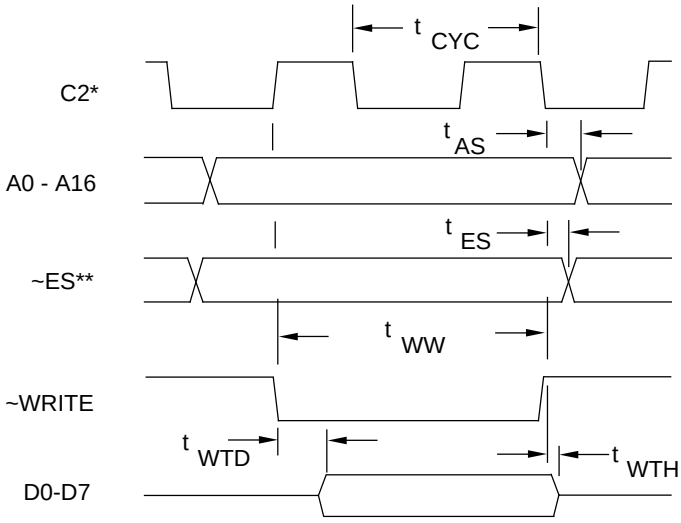
1. Internal operating frequency = 52.416 MHz/2 = 26.208 MHz.
2. ES = ~RAMSEL or ~ROMSEL.
3. t_{RW}, t_{WW} = 1.5 t_{CYC}



* C2 = Internal Phase 2 clock.

** ~ES = ~RAMSEL or ~ROMSEL.

Read Timing



* C2 = Internal Phase 2 clock.

** ~ES = ~RAMSEL or ~ROMSEL.

Write Timing

1046F3-5 EB WF

Figure 3-5. Waveforms - External Memory Bus

3.2.2 Parallel Host Bus Timing

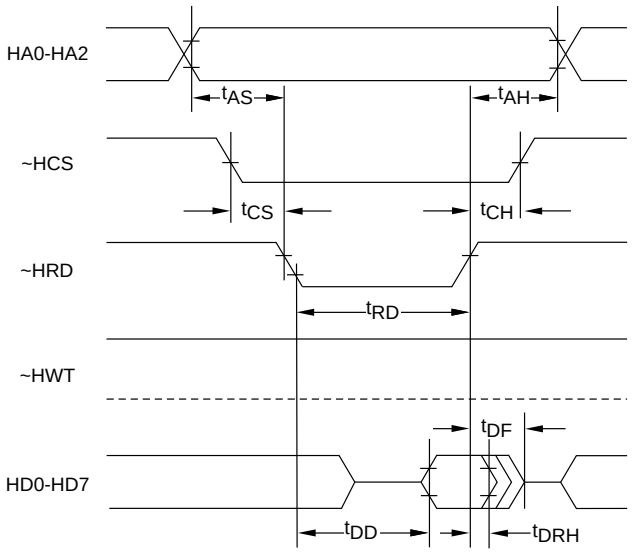
The parallel host bus timing is listed in Table 3-9 and illustrated in Figure 3-11.

Table 3-9. Timing - Parallel Host Bus

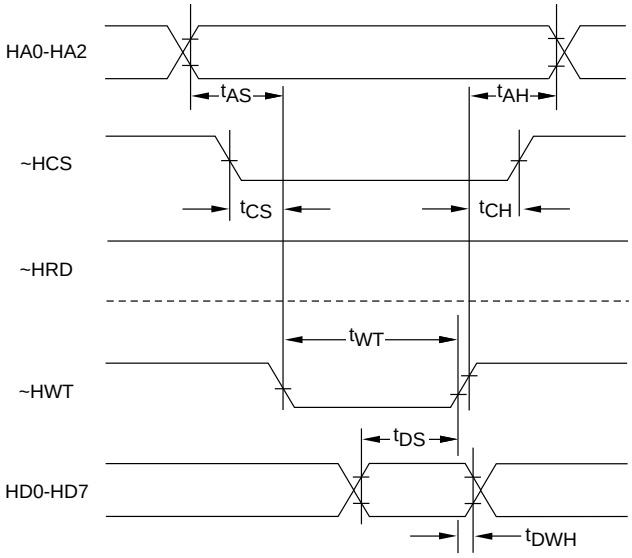
Symbol	Parameter	Min	Max	Units
	READ (See Notes 1,2, and 3)			
t_{AS}	Address Setup	7	–	ns
t_{AH}	Address Hold	10	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{RD}	~HRD Strobe Width	51	–	ns
t_{DD}	Read Data Delay	–	45	ns
t_{DRH}	Read Data Hold	10	–	ns
	WRITE (See Notes 1,2, and 3)			
t_{AS}	Address Setup	7	–	ns
t_{AH}	Address Hold	10	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{WT}	~HWT Strobe Width	51	–	ns
t_{DS}	Write Data Setup	5	–	ns
t_{DWH}	Write Data Hold	5	–	ns

Notes:

1. When the host executes consecutive Rx FIFO reads, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (215 ns at 10 MHz) is required from the falling edge of ~HRD to the falling edge of the next Host Rx FIFO ~HRD clock.
2. When the Host executes consecutive Tx FIFO writes, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (215 ns at 10 MHz) is required from the falling edge of ~HWT to the falling edge of the next Host Tx FIFO ~HWT clock.
3. t_{RD}, t_{WT} = t_{CYC} + 12 ns



a. Host Read



b. Host Write

876F3-8 HB WF

Figure 3-6. Waveforms - Parallel Host Bus

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4. PARALLEL HOST INTERFACE

The modem supports a 16550A interface in parallel interface versions. The 16550A interface can operate in FIFO mode or non-FIFO mode. Non-FIFO mode is the same as 16450 interface operation. FIFO mode unique operations are identified.

4.1 OVERVIEW

Table 4-1 shows the parallel interface registers and the corresponding bit assignments.

The modem emulates the 16450/16550A interface and includes both a 16-byte receiver data first-in first-out buffer (RX FIFO) and a 16-byte transmit data first-in first-out buffer (TX FIFO). When FIFO mode is selected in the FIFO Control Register (FCR0 = 1), both FIFOs are operative. Furthermore, when FIFO mode is selected, DMA operation of the FIFO can also be selected (FCR3 = 1). When FIFO mode is not selected, operation is restricted to 16450 interface operation.

The received data is read by the host from the Receiver Buffer (RX Buffer). The RX Buffer corresponds to the Receiver Buffer Register in a 16550A device. In FIFO mode, the RX FIFO operates transparently behind the RX Buffer. Interface operation is described with reference to the RX Buffer in both FIFO and non-FIFO modes.

The transmit data is loaded by the host into the Transmit Buffer (TX Buffer). The TX Buffer corresponds to the Transmit Holding Register in a 16550A device. In FIFO mode, the TX FIFO operates transparently behind the TX Buffer. Interface operation is described with reference to the TX Buffer in both FIFO and non-FIFO modes.

Table 4-1. Parallel Interface Registers

Register No.	Register Name	Bit No. 7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	RX FIFO Error	Transmitter Empty (TEMT)	Transmitter Buffer Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Receiver Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Local Loopback	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	Interrupt Identify Register (IIR) (Read Only)	FIFOs Enabled	FIFOs Enabled	0	0	Pending Interrupt ID Bit 2	Pending Interrupt ID Bit 1	Pending Interrupt ID Bit 0	"0" if Interrupt Pending
2	FIFO Control Register (FCR) (Write Only)	Receiver Trigger MSB	Receiver Trigger LSB	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
1 (DLAB = 0)	Interrupt Enable Register (IER)	0	0	0	0	Enable Modem Status Interrupt (EDSSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Enable Received Data Available Interrupt (ERBFI)
0 (DLAB = 0)	Transmitter Buffer Register (THR)	Transmitter FIFO Buffer Register (Write Only)							
0 (DLAB = 0)	Receiver Buffer Register (RBR)	Receiver FIFO Buffer Register (Read Only)							
1 (DLAB = 1)	Divisor Latch MSB Register (DLM)	Divisor Latch MSB							
0 (DLAB = 1)	Divisor Latch LSB Register (DLL)	Divisor Latch LSB							

4.2 REGISTER SIGNAL DEFINITIONS

4.2.1 IER - Interrupt Enable Register (Addr = 1, DLAB = 0)

The IER enables five types of interrupts that can separately assert the HINT output signal (Table 4-2). A selected interrupt can be enabled by setting the corresponding enable bit to a 1, or disabled by setting the corresponding enable bit to a 0. Disabling an interrupt in the IER prohibits setting the corresponding indication in the IIR and assertion of HINT. Disabling all interrupts (resetting IER0 - IER3 to a 0) inhibits setting of any Interrupt Identifier Register (IIR) bits and inhibits assertion of the HINT output. All other system functions operate normally, including the setting of the Line Status Register (LSR) and the Modem Status Register (MSR).

Bits 7-4 Not used.

Always 0.

Bit 3 Enable Modem Status Interrupt (EDSSI).

This bit, when a 1, enables assertion of the HINT output whenever the Delta CTS (MSR0), Delta DSR (MSR1), Delta TER (MSR2), or Delta DCD (MSR3) bit in the Modem Status Register (MSR) is a 1. This bit, when a 0, disables assertion of HINT due to setting of any of these four MSR bits.

Bit 2 Enable Receiver Line Status Interrupt (ELSI).

This bit, when a 1, enables assertion of the HINT output whenever the Overrun Error (LSR1), Parity Error (LSR2), Framing Error (LSR3), or Break Interrupt (LSR4) receiver status bit in the Line Status Register (LSR) changes state. This bit, when a 0, disables assertion of HINT due to change of the receiver LSR bits 1-4.

Bit 1 Enable Transmitter Holding Register Empty Interrupt (ETBEI).

This bit, when a 1, enables assertion of the HINT output when the Transmitter Empty bit in the Line Status Register (LSR5) is a 1. This bit, when a 0, disables assertion of HINT due to LSR5.

Bit 0 Enable Receiver Data Available Interrupt (ERBFI) and Character Timeout in FIFO Mode.

This bit, when a 1, enables assertion of the HINT output when the Receiver Data Ready bit in the Line Status Register (LSR0) is a1 or character timeout occurs in the FIFO mode. This bit, when a 0, disables assertion of HINT due to the LSR0 or character timeout.

4.2.2 FCR - FIFO Control Register (Addr = 2, Write Only)

The FCR is a write-only register used to enable FIFO mode, clear the RX FIFO and TX FIFO, enable DMA mode, and set the RX FIFO trigger level.

Bits 7-6 RX FIFO Trigger Level.

FCR7 and FCR6 set the trigger level for the RX FIFO (Receiver Data Available) interrupt.

FCR7	FCR6	RX FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Bits 5-4 Not used.

Bit 3 DMA Mode Select.

When FIFO mode is selected (FCR0 = 1), FCR3 selects non-DMA operation (FCR3 = 0) or DMA operation (FCR3 = 1). When FIFO mode is not selected (FCR0 = 0), this bit is not used (the modem operates in non-DMA mode in 16450 operation).

DMA operation in FIFO mode.

RXRDY will be asserted when the number of characters in the RX FIFO is equal to or greater than the value in the RX FIFO Trigger Level (IIR0-IIR3 = 4h) or the received character timeout (IIR0-IIR3 = Ch) has occurred. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there are one or more empty (unfilled) locations in the TX FIFO. TXRDY will go inactive when the TX FIFO is completely full.

Non-DMA operation in FIFO mode.

RXRDY will be asserted when there are one or more characters in the RX FIFO. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there are no characters in the TX FIFO. TXRDY will go inactive when the first character is loaded into the TX FIFO Buffer.

Bit 2 TX FIFO Reset.

When FCR2 is a 1, all bytes in the TX FIFO are cleared. This bit is cleared automatically by the modem.

Bit 1 RX FIFO Reset.

When FCR1 is a 1, all bytes in the RX FIFO are cleared. This bit is cleared automatically by the modem.

Bit 0 FIFO Enable.

When FCR0 is a 0, 16450 mode is selected and all bits are cleared in both FIFOs. When FCR0 is a 1, FIFO mode (16550A mode) is selected and both FIFOs are enabled. FCR0 must be a 1 when other bits in the FCR are written or they will not be acted upon.

4.2.3 IIR - Interrupt Identifier Register (Addr = 2)

The Interrupt Identifier Register (IIR) identifies the existence and type of up to five prioritized pending interrupts. Four priority levels are set to assist interrupt processing in the host. The four levels, in order of decreasing priority, are: Highest: Receiver Line Status, 2: Receiver Data Available or Receiver Character Timeout, 3: TX Buffer Empty, and 4: Modem Status.

When the IIR is accessed, the modem freezes all interrupts and indicates the highest priority interrupt pending to the host. Any change occurring in interrupt conditions are not indicated until this access is complete.

Bits 7-6 FIFO Mode.

These two bits copy FCR0.

Bits 5-4 Not Used.

Always 0.

Bits 3-1 Highest Priority Pending Interrupt.

These three bits identify the highest priority pending interrupt (Table 4-2). Bit 3 is applicable only when FIFO mode is selected, otherwise bit 3 is a 0.

Bit 0 Interrupt Pending.

When this bit is a 0, an interrupt is pending; IIR bits 1-3 can be used to determine the source of the interrupt. When this bit is a1, an interrupt is not pending.

Table 4-2. Interrupt Sources and Reset Control

Interrupt Identification Register					Interrupt Set and Reset Functions		
Bit 3 (Note 1)	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error OE (LSR1), Parity Error (PE) (LSR2), Framing Error (FE) (LSR3), or Break Interrupt (BI) (LSR4)	Reading the LSR
0	1	0	0	2	Received Data Available	Received Data Available (LSR0) or RX FIFO Trigger Level (FCR6-FCR7) Reached[1]	Reading the RX Buffer or the RX FIFO drops below the Trigger Level
1	1	0	0	2	Character Time-out Indication [1]	The RX FIFO contains at least 1 character and no characters have been removed from or input to the RX FIFO during the last 4 character times.	Reading the RX Buffer
0	0	1	0	3	TX Buffer Empty	TX Buffer Empty	Reading the IIR or writing to the TX Buffer
0	0	0	0	4	Modem Status	Delta CTS (DCTS) (MSR0), Delta DSR (DDSR) (MSR1), Trailing Edge Ring Indicator (TERI) (MSR3), or Delta DCD (DCD) (MSR4)	Reading the MSR

Notes:
1. FIFO Mode only.

4.2.4 LCR - Line Control Register (Addr = 3)

The Line Control Register (LCR) specifies the format of the asynchronous data communications exchange.

Bit 7 **Divisor Latch Access Bit (DLAB).**

This bit must be set to a 1 to access the Divisor latch registers during a read or write operation. It must be reset to a 0 to access the Receiver Buffer, the Transmitter Buffer, or the Interrupt Enable Register.

Bit 6 **Set Break.**

When bit 6 is a 1, the transmit data is forced to the break condition, i.e., space (0) is sent. When bit 6 is a 0, break is not sent. The Set Break bit acts only on the transmit data and has no effect on the serial in logic.

Bit 5 **Stick Parity.**

When parity is enabled (LCR3 = 1) and stick parity is selected (LCR5 = 1), the parity bit is transmitted and checked by the receiver as a 0 if even parity is selected (LCR4 = 1) or as a 1 if odd parity is selected (LCR4 = 0). When stick parity is not selected (LCR3 = 0), parity is transmit and checked as determined by the LCR3 and LCR4 bits.

Bit 4 **Even Parity Select (EPS).**

When parity is enabled (LCR3 = 1) and stick parity is not selected (LCR5 = 0), the number of 1s transmitted or checked by the receiver in the data word bits and parity bit is either even (LCR4 = 1) or odd (LCR4 = 0).

Bit 3 **Enable Parity (PEN).**

When bit 3 is a 1, a parity bit is generated in the serial out (transmit) data stream and checked in the serial in (receive) data stream as determined by the LCR 4 and LCR5 bits. The parity bit is located between the last data bit and the first stop bit.

Bit 2 **Number of Stop Bits (STB).**

This bit specifies the number of stop bits in each serial out character. If bit 2 is a 0, one stop bit is generated regardless of word length. If bit 2 is a 1 and 5-bit word length is selected, one and one-half stop bits are generated. If bit 2 is a 1 and a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The serial in logic checks the first stop bit only, regardless of the number of stop bits selected.

Bits 1-0 **Word Length Select (WLS0 and WLS1).**

These two bits specify the number of bits in each serial in or serial out character. The encoding of bits 0 and 1 is:

Bit 1	Bit 0	Word Length
0	0	5 Bits (Not supported)
0	1	6 Bits (Not supported)
1	0	7 Bits
1	1	8 Bits

4.2.5 MCR - Modem Control Register (Addr = 4)

The Modem Control Register (MCR) controls the interface with the modem or data set.

Bit 7-5 **Not used.**

Always 0.

Bit 4 **Local Loopback.**

When this bit is set to a 1, the diagnostic mode is selected and the following occurs:

1. Data written to the Transmit Buffer is looped back to the Receiver Buffer.
2. The DTS (MCR0), RTS (MCR1), Out1 (MCR2), and Out2 (MCR3) modem control register bits are internally connected to the DSR (MSR5), CTS (MSR4), RI (MSR6), and DCD (MSR7) modem status register bits, respectively.

Bit 3 **Output 2.**

When this bit is a 1, HINT is enabled. When this bit is a 0, HINT is in the high impedance state.

Bit 2 **Output 1.**

This bit is used in local loopback (see MCR4).

Bit 1 **Request to Send (RTS).**

This bit controls the Request to Send (RTS) function. When this bit is a 1, RTS is on. When this bit is a 0, RTS is off.

Bit 0 **Data Terminal Ready (DTR).**

This bit controls the Data Terminal Ready (DTR) function. When this bit is a 1, DTR is on. When this bit is a 0, DTR is off.

4.2.6 LSR - Line Status Register (Addr = 5)

This 8-bit register provides status information to the host concerning data transfer.

Bit 7 **RX FIFO Error.**

In the 16450 mode, this bit is not used and is always 0.

In the FIFO mode, this bit is set if there are one or more characters in the RX FIFO with a parity error, framing error, or break indication detected. This bit is reset to a 0 when the host reads the LSR and none of the above conditions exist in the RX FIFO.

Bit 6 **Transmitter Empty (TEMT).**

This bit is set to a 1 whenever the TX Buffer (THR) and equivalent of the Transmitter Shift Register (TSR) are both empty. It is reset to a 0 whenever either the THR or the equivalent of the TSR contains a character.

In the FIFO mode, this bit is set to a 1 when ever the TX FIFO and the equivalent of the TSR are both empty.

Bit 5 **Transmitter Holding Register Empty (THRE) [TX Buffer Empty].**

This bit, when set, indicates that the TX Buffer is empty and the modem can accept a new character for transmission. In addition, this bit causes the modem to issue an interrupt to the host when the Transmit Holding Register Empty Interrupt Enable bit (IIR1) is set to 1. The THRE bit is set to a 1 when a character is transferred from the TX Buffer. The bit is reset to 0 when a byte is written into the TX Buffer by the host.

In the FIFO mode, this bit is set when the TX FIFO is empty; it is cleared when at least one byte is in the TX FIFO.

Bit 4 **Break Interrupt (BI).**

This bit is set to a 1 whenever the received data input is a space (logic 0) for longer than two full word lengths plus 3 bits. The BI bit is reset when the host reads the LSR.

Bit 3 **Framing Error (FE).**

This bit indicates that the received character did not have a valid stop bit. The FE bit is set to a 1 whenever the stop bit following the last data bit or parity bit is detected as a logic o (space). The FE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, the error indication is associated with the particular character in the FIFO it applies to; the FE bit is set to a 1 when this character is loaded into the RX Buffer.

Bit 2 **Parity Error (PE).**

This bit indicates that the received data character in the RX Buffer does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR4) and the Stick Parity bit (LCR5). The PE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, the error indication is associated with the particular character in the it applies to; the PE bit is set to a 1 when this character is loaded into the RX Buffer.

Bit 1 **Overrun Error (OE).**

This bit is set to a 1 whenever received data is loaded into the RX Buffer before the host has read the previous data from the RX Buffer. The OE bit is reset to a 0 when the host reads the LSR.

In the FIFO mode, if data continues to fill beyond the trigger level, an overrun condition will occur only if the RX FIFO is full and the next character has been completely received.

Bit 0 **Receiver Data Ready (DR).**

This bit is set to a 1 whenever a complete incoming character has been received and has been transferred into the RX Buffer. The DR bit is reset to a 0 when the host reads the RX Buffer.

In the FIFO mode, the DR bit is set when the number of received data bytes in the RX FIFO equals or exceeds the trigger level specified in FCR0-FCR1.

4.2.7 MSR - Modem Status Register (Addr = 6)

The Modem Status Register (MSR) reports current state and change information of the modem. Bits 4-7 supply current state and bits 0-3 supply change information. The change bits are set to a 1 whenever a control input from the modem changes state from the last MSR read by the host. Bits 0-3 are reset to 0 when the host reads the MSR or upon reset.

Whenever Bits 0, 1, 2, or 3 are set to a 1, a Modem Status Interrupt (IIR0-IIR3 = 0) is generated.

Bit 7 **Data Carrier Detect (DCD).**

This bit indicates the logic state of the ~DCD (~RLSD) output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the Out2 bit in the MCR (MCR3).

Bit 6 **Ring Indicator (RI).**

This bit indicates the logic state of the ~RI output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the Out1 bit in the MCR (MCR2).

Bit 5 **Data Set Ready (DSR).**

This bit indicates the logic state of the ~DSR output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the DTR bit in the MCR (MCR0).

Bit 4 **Clear to Send (CTS).**

This bit indicates the logic state of the ~CTS output. If Loopback is selected (MCR4 = 1), this bit reflects the state of the RTS bit in the MCR (MCR1).

Bit 3 **Delta Data Carrier Detect (DDCD).**

This bit is set to a 1 when the DCD bit changes state since the MSR was last read by the host.

Bit 2 **Trailing Edge of Ring Indicator (TERI).**

This bit is set to a 1 when the RI bit changes from a 1 to a 0 state since the MSR was last read by the host.

Bit 1 **Delta Data Set Ready (DDSR).**

This bit is set to a 1 when the DSR bit has changed since the MSR was last read by the host.

Bit 0 **Delta Clear to Send (DCTS).**

This bit is set to a 1 when the CTS bit has changed since the MSR was last read by the host.

4.2.8 RBR - RX Buffer (Receiver Buffer Register) (Addr = 0, DLAB = 0)

The RX Buffer (RBR) is a read-only register at location 0 (with DLAB = 0). Bit 0 is the least significant bit of the data, and is the first bit received.

4.2.9 THR - TX Buffer (Transmitter Holding Register) (Addr = 0, DLAB = 0)

The TX Buffer (THR) is a write-only register at address 0 when DLAB = 0. Bit 0 is the least significant bit and the first bit sent.

4.2.10 Divisor Registers (Addr = 0 and 1, DLAB = 1)

The Divisor Latch LS (least significant byte) and Divisor Latch MS (most significant byte) are two read-write registers at locations 0 and 1 when DLAB = 1, respectively.

The baud rate is selected by loading each divisor latch with the appropriate hex value.

Programmable values corresponding to the desired baud rate are listed in Table 4-3.

4.2.11 SCR - Scratch Register (Addr = 7)

The Scratchpad Register is a read-write register at location 7. This register is not used by the modem and can be used by the host for temporary storage.

Table 4-3. Programmable Baud Rates

Divisor Latch (Hex)			
MS	**LS**	**Divisor (Decimal)**	**Baud Rate**
06	00	1536	75
04	17	1047	110
03	00	768	150
01	80	384	300
00	C0	192	600
00	60	96	1200
00	30	48	2400
00	18	24	4800
00	0C	12	9600
00	06	6	19200
00	04	4	28800
00	03	3	38400
00	02	2	57600
00	01	1	115200

Note: Values correspond to a UART input frequency of 1.8432 MHz.

4.3 RECEIVER FIFO INTERRUPT OPERATION

4.3.1 Receiver Data Available Interrupt

When the FIFO mode is enabled (FCR0 = 1) and receiver interrupt (RX Data Available) is enabled (IER0 = 1), receiver interrupt operation is as follows:

1. The Receiver Data Available Flag (LSR0) is set as soon as a received data character is available in the RX FIFO. LSR0 is cleared when the RX FIFO is empty.
2. The Receiver Data Available interrupt code (IIR0-IIR4 = 4h) is set whenever the number of received data bytes in the RX FIFO reaches the trigger level specified by FCR6-FCR7 bits; it is cleared whenever the number of received data bytes in the RX FIFO drops below the trigger level specified by FCR6-FCR7 bits.
3. The HINT interrupt is asserted whenever the number of received data bytes in the RX FIFO reaches the trigger level specified by FCR6-FCR7 bits. HINT interrupt is de-asserted when the number of received data bytes in the RX FIFO drops below the trigger level specified by FCR6-FCR7 bits.

4.3.2 Receiver Character Timeout Interrupts

When the FIFO mode is enabled (FCR0 = 1) and receiver interrupt (Receiver Data Available) is enabled (IER0 = 1), receiver character timeout interrupt operation is as follows:

1. A Receiver character timeout interrupt code (IIR0-IIR3 = Ch) is set if at least one received character is in the RX FIFO, the most recent received serial character was longer than four continuous character times ago (if 2 stop bits are specified, the second stop bit is included in this time period), and the most recent host read of the RX FIFO was longer than four continuous character times ago.

4.4 TRANSMITTER FIFO INTERRUPT OPERATION

4.4.1 Transmitter Empty Interrupt

When the FIFO mode is enabled (FCR0 = 1) and transmitter interrupt (TX Buffer Empty) is enabled (IER0 = 1), transmitter interrupt operation is as follows:

1. The TX Buffer Empty interrupt code (IIR0-IIR3 = 2h) will occur when the TX Buffer is empty; it is cleared when the TX Buffer is written to (1 to 16 characters)or the IIR is read.
2. The TX Buffer Empty indications will be delayed 1 character time minus the last stop bit time whenever the following occur: THRE = 1 and there have not been at least two bytes at the same time in the TX FIFO Buffer since the last setting of THRE was set. The first transmitter interrupt after setting FCR0 will be immediate.

5. DESIGN CONSIDERATIONS

Good engineering practices must be followed when designing a printed circuit board (PCB) containing the modem device. This is especially important considering the high data bit rate, high fax rate, record/play of analog speech and music audio, and full-duplex speakerphone operation. Suppression of noise is essential to the proper operation and performance of the modem and interfacing audio and DAA circuits.

Two aspects of noise in an OEM board design containing the modem device set must be considered: on-board/off-board generated noise that can affect analog signal levels and analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC), and on-board generated noise that can radiate off-board. Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality, especially in low level analog signals. Of particular concern is noise in frequency ranges affecting modem and audio circuit performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met for use in specific environments. In order to minimize the contribution of the circuit design and PCB layout to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

Proper PC board layout (component placement and orientation, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to attain EMI certification.

All the aspects of proper engineering practices are beyond the scope of this designer's guide. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

The following guidelines are offered to specifically help achieve stated modem performance, minimize audible noise for audio circuit use, and to minimize EMI generation.

5.1 PC BOARD LAYOUT GUIDELINES

5.1.1 General Principles

1. Provide separate digital, analog, and DAA sections on the board.
2. Keep digital and analog components and their corresponding traces as separate as possible and confined to defined sections.
3. Keep high speed digital traces as short as possible.
4. Keep sensitive analog traces as short as possible.
5. Provide proper power supply distribution, grounding, and decoupling.
6. Provide separate digital ground, analog ground, and chassis ground (if appropriate) planes.
7. Provide wide traces for power and critical signals.
8. Position digital circuits near the host bus or serial DTE connection and position the DAA circuits near the telephone line connections.

5.1.2 Component Placement

1. From the system circuit schematic,
   a) Identify the digital, analog, and DAA circuits and their components, as well as external signal and power connections.
   b) Identify the digital, analog, mixed digital/analog components within their respective circuits.
   c) Note the location of power and signals pins for each device (IC).
2. Roughly position digital, analog, and DAA circuits on separate sections of the board. Keep the digital and analog components and their corresponding traces as separate as possible and confined to their respective sections on the board. Typically, the digital circuits will cover one-half of the board, analog circuits will cover one-fourth of the board, and the DAA will cover one-fourth of the board. **NOTE:** While the DAA is primarily analog in nature, it also has many control

and status signals routed through it. A DAA section is also governed by local government regulations covering subjects such as component spacing, high voltage suppression, and current limiting.

3. Once sections have been roughly defined, place the components starting with the connectors and jacks.
   a) Allow sufficient clearance around connectors and jacks for mating connectors and plugs.
   b) Allow sufficient clearance around components for power and ground traces.
   c) Allow sufficient clearance around sockets to allow the use of component extractors.
4. First, place the mixed analog/digital components (e.g., modem device, A/D converter, and D/A converter).
   a) Orient the components so pins carrying digital signals extend onto the digital section and pins carrying analog signals extend onto the analog section as much as possible.
   b) Position the components to straddle the border between analog and digital sections.
5. Place all analog components.
   a) Place the analog circuitry, including the DAA, on the same area of the PCB.
   b) Place the analog components close to and on the side of board containing the TXA1, TXA2, RIN, VC, and VREF signals.
   c) Avoid placing noisy components and traces near TXA1, TXA2, RIN, VC, and VREF lines.
   d) For serial DTE models, place receivers and drivers for DTE EIA/TIA-232-E serial interface signals close to the connectors and away from traces carrying high frequency clocks in order to avoid/minimize the addition of noise suppression components (i.e., chokes and capacitors) for each line.
6. Place active digital components/circuits and decoupling capacitors.
   a) Place digital components close together in order to minimize signal trace length.
   b) Place 0.1 µF decoupling (bypass) capacitors close to the pins (usually power and ground) of the IC they are decoupling. Make the smallest loop area possible between the capacitor and power/ground pins to reduce EMI.
   c) For parallel host bus models, place host bus interface components close to the edge connector in accordance with the applicable bus interface standard, e.g., use a 2.5-in maximum trace length for ISA bus.
   d) For serial DTE models, place serial DTE interface components near the DTE connector.
   e) Place crystal circuits as close as possible to the devices they drive.
7. Provide a "connector" component, usually a zero ohm resistor or a ferrite bead at one or more points on the PCB to connect one section's ground to another.

5.1.3 Signal Routing

1. Route the modem signals to provide maximum isolation between noise sources and noise sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The modem noise source, neutral, and noise sensitive pins are listed in Table 5-1.
2. Keep digital signals within the digital section and analog signals within the analog section. (Previous placement of isolation traces should prevent these traces from straying outside their respective sections.) Route the digital traces perpendicular to the analog traces to minimize signal cross coupling.
3. Provide isolation traces (usually ground traces) to ensure that analog signals are confined to the analog section and digital traces remain out of the analog section. A trace may have to be narrowed to route it though a mixed analog/digital IC, but try to keep the trace continuous.
   a) Route an analog isolation ground trace, at least 50 mil to 100 mil wide, around the border of the analog section; put on both sides of the PCB.
   b) Route a digital isolation ground trace, at least 50 mil to 100 mil wide, and 200 mil wide on one side of the PCB edge, around the border of the digital section.
4. Keep host interface signals (e.g., ~HCS, ~HRD, ~HWT, and ~RESET) traces at least 10 mil thick (preferably 12 - 15 mil).

5. Keep analog signal (e.g., MICM, MICV, SPKV, VC, VREF, TXA1, TXA2, RXA, TELIN, and TELOUT) traces at least 10 mil thick (preferably 12 - 15 mil).
6. Keep all other signal traces as wide as possible, at least 5 mil (preferably 10 mil). Route the signals between components by the shortest possible path (the components should have been previously placed to allow this).
7. Route the traces between bypass capacitors to IC pins, at least 25 mil wide; avoid vias if possible.
8. Gather signals that pass between sections (typically low speed control and status signals) together and route them between sections through a path in the isolation ground traces at one (preferred) or two points only. If the path is made on one side only, then the isolation trace can be kept contiguous by briefly passing it to the other side of the PCB to jump over the signal traces.
9. Avoid right angle (90 degree) turns on high frequency traces. Use smoothed radiuses or 45 degree corners.
10. Minimize the number of through-hole connections (feedthroughs/vias) on traces carrying high frequency signals.
11. Keep all signal traces away from crystal circuits.
12. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.
13. Provide adequate clearance (e.g., 60 mil minimum) around feedthroughs in any internal planes in the DAA circuit.
14. Eliminate ground loops, which are unexpected current return paths to the power source.

Table 5-1. Modem Pin Noise Characteristics

Device	Function	Noise Source	Neutral	Noise Sensitive
Serial Interface	VDD		31, 38	
	GND, AGND		34, 37	
	Crystal	52-53		
	Reset Control		35	
	External Memory Bus	1-6, 9-10, 12-13, 43-50, 58-68		
	NVRAM		39, 42	
	Telephone Line Interface		7-8, 36, 51, 54	24-25, 30, 32-33
	Audio Interface			23, 26-29
	Serial DTE/Indicator Interface	40-41	11, 14-22, 55-57	
Parallel Interface	VDD		31, 38	
	GND, AGND		34, 37	
	Crystal	52-53		
	Reset Control		35	
	External Memory Bus	1-6, 9-10, 12-13, 43-50, 58-68		
	NVRAM		39, 42	
	Telephone Line Interface		7-8, 36, 51, 54	24-25, 30, 32-33
	Audio Interface			23, 26-29
	Parallel Host Bus Interface	11, 14-22, 40-41, 55-57		

5.1.4 Power

1. Identify power supply (VDD) connections.
2. Place a 10 µF electrolytic or tantalum capacitor in parallel with a ceramic 0.1 µF capacitor between power and ground at one or more points in the digital section. Place one set nearest to where power enters the PCB (edge connector or power connector) and place another set at the furthest distance from where power enters the PCB. These capacitors help to supply current surge demands by the digital circuits and prevent those surges from generating noise on the power lines that may affect other circuits.
3. For 2-layer boards, route a 200-mil wide power trace on two edges of the same side of the PCB around the border of the circuits using the power. (Note that a digital ground trace should likewise be routed on the other side of the board.)
4. Generally, route all power traces before signal traces.

5.1.5 Ground Planes

1. In a 2-layer design, provide digital and analog ground plane areas in all unused space around and under digital and analog circuit components (exclusive of the DAA), respective, on both sides of the board, and connect them such a manner as to avoid small islands. Connect each ground plane area to like ground plane areas on the same side at several points and to like ground plane areas on the opposite side through the board at several points. Connect all modem DGND pins to the digital ground plane area and AGND pins to the analog ground plane area. Typically, separate the collective digital ground plane area from the collective analog ground plane area by a fairly straight gap. There should be no inroads of digital ground plane area extending into the analog ground plane area or visa versa.
2. In a 4-layer design, provide separate digital and analog ground planes covering the corresponding digital and analog circuits (exclusive of the DAA), respectively. Connect all modem DGND pins to the digital ground plane and AGND pins to the analog ground plane. Typically, separate the digital ground plane from the analog ground plane by a fairly straight gap.
3. In a design which needs EMI filtering, define an additional "chassis" section adjacent to the bracket end of a plug-in card. Most EMI components (usually ferrite beads/capacitor combinations) can be positioned in this section. Fill the unused space with a chassis ground plane, and connect it to the metal card bracket and any connector shields/grounds.
4. Keep the current paths of separate board functions isolated, thereby reducing the current's travel distance. Separate board functions are: host interface, display, digital (SRAM, EPROM, modem), and DAA. Power and ground for each of these functions should be separate islands connected together at the power and ground source points only.
5. For serial DTE models, decouple the power cord at the power cord interface with decoupling capacitors. Methods to decouple power lines are similar to decoupling telephone lines.
6. Connect grounds together at only one point, if possible, using a ferrite bead. Allow other points for grounds to be connected together if necessary for EMI suppression. For ISA bus board design, include a zero ohm resistor between digital ground and the PC mounting bracket to allow connecting digital ground to the bracket if needed.
7. Keep all ground traces as wide as possible, at least 25 mil to 50 mil.
8. Keep the traces connecting all decoupling capacitors to power and ground at their respective ICs as short and as direct (i.e., not going through vias) as possible.

5.1.6 Crystal Circuit

1. Keep all traces and component leads connected to crystal input and output pins (i.e., XTLI and XTLO) short in order to reduce induced noise levels and minimize any stray capacitance that could affect the crystal oscillator. Keep the XTLO trace extremely short with no bends greater than 45 degrees and containing no vias since the XTLO pin is connected to a fast rise time, high current driver.
2. Where a ground plane is not available, such as in a 2-layer design, tie the crystal capacitors ground paths using separate short traces (as wide as possible) with minimum angles and vias directly to the corresponding device digital ground pin nearest the crystal pins.
3. Connect crystal cases(s) to ground (if applicable).
4. Place a 100-ohm (typical) resistor between the XTLO pin and the crystal/capacitor node.
5. Connect crystal capacitor ground connections directly to GND pin on the modem device. Do not use common ground plane or ground trace to route the capacitor GND pin to the corresponding modem GND pin.

5.1.7 Standalone Modem Design with EIA/TIA-232 Interface

1. Use a metal enclosure. If a plastic enclosure is required, line the internal enclosure with metal foil or apply conductive spray to the top and bottom covers to reduce emissions.
2. Place a common mode choke in series with each power supply line.
3. Place components close to each other and close to the EIA/TIA-232 interface cable connector.
4. Connect power and ground for all EIA/TIA-232 components to the power and ground source points via separate power and ground traces that are not connected to the digital power and ground "except" at these source points. Power and ground source points are the board input pins or a regulator output if used.
5. Connect the EIA/TIA-232 cable signal ground wire to digital ground.
6. Terminate the EIA/TIA-232 cable shield at the modem enclosure in one of the following manners as needed to minimize RF emissions: leave open, connect to digital ground through a ferrite bead, or connect directly to digital ground and provide a ferrite toroid around the EIA/TIA-232 cable close to the modem enclosure.

5.1.8 VC and VREF Circuit

1. Provide extremely short, independent paths for VC and VREF capacitor connections.
   a) Route the connection from the plus terminal of the 10 µF VC capacitor and one terminal of the 0.1 µF VC capacitor to the modem device VC pin (pin 24) using a single trace isolated from the trace to the VC pin from the VREF capacitors (see step d).
   b) Route the connection from the negative terminal of the 10 µF VC capacitor and the other terminal of a the 0.1 µF VC capacitor to a ferrite bead. The bead should typically have characteristics such as: impedance = 70 Ω at a frequency of 100 MHz , rated current = 200 mA, and maximum resistance = 0.5 Ω. Connect the other bead terminal to the AGND pin (pin 34) with a single trace.
   c) Route the connection from the plus terminal of the 10 µF VREF capacitor and one terminal of the 0.1 µF VREF capacitor to the modem device VREF pin (pin 25) with a single trace.
   d) Route the connection from the negative terminal of 10 µF VREF capacitor and the other terminal of the 0.1 µF VREF capacitor to the modem device VC pin (pin 24) with a single trace isolated from the trace to the VC pin from the VC capacitors (see step a).

5.1.9 Telephone and Local Handset Interface

1. Place common mode chokes in series with Tip and Ring for each connector.
2. Decouple the telephone line cables at the telephone line jacks. Typically, use a combination of series inductors, common mode chokes, and shunt capacitors. Methods to decouple telephone lines are similar to decoupling power lines, however, telephone line decoupling may be more difficult and deserves additional attention. A commonly used design aid is to place footprints for these components and populate as necessary during performance/EMI testing and certification.
3. Place high voltage filter capacitors (.001 µF @1KV) from Tip and Ring to digital ground.

5.1.10 Optional Configurations

Because fixed requirements of a design may alter EMI performance, guidelines that work in one case may deliver little or no performance enhancement in another. Initial board design should, therefore, include flexibility to allow evaluation of optional configurations. These optional configurations may include:

1. Chokes in Tip and Ring lines replaced with jumper wires as a cost reduction if the design has sufficient EMI margin.
2. Various grounding areas connected by tie points (these tie points can be short jumper wires, solder bridges between close traces, etc.).
3. EIA/TIA-232 cable ground wire or cable shielding connected on the board or floated.
4. Develop two designs in parallel; one based on a 2-layer board and the other based on a 4-layer board. During the evaluation phase, better performance of one design over another may result in quicker time to market.

5.2 CRYSTAL SPECIFICATIONS

The specifications and recommended suppliers for crystals are listed in Table 5-2.

Table 5-2. Crystal Specifications - 52.416 MHz

Characteristic	Value	Value
Rockwell Part No.	333R45-008	5333R04-013
Electrical		
Frequency	52.416 MHz nom.	52.416 MHz nom.
Frequency Tolerance	±40 ppm (C_L = 16.5 and 19.5 pF)	±50 ppm (C_L = 16.5 and 19.5 pF)
Frequency Stability		
vs. Temperature	±45 ppm (0°C to 70°C)	±35 ppm (0°C to 70°C)
vs. Aging	±15 ppm/5 years	±15 ppm/4 years
Oscillation Mode	Third overtone	Third overtone
Calibration Mode	Parallel resonant	Parallel resonant
Load Capacitance, C_L	18 pF nom.	18 pF nom.
Shunt Capacitance, C_O	6 pF max.	7 pF max.
Series Resistance, R_1	35 Ω max. @20 nW drive level	80 Ω max. @20 nW drive level
Drive Level	100µW correlation; 500µW max.	100µW correlation; 300µW max.
Operating Temperature	0°C to 70°C	0°C to 70°C
Storage Temperature	–40°C to 85°C	–30°C to 80°C
Mechanical		
Dimensions (L x W x H)	11.05 x 4.65 x 13.46 mm	7.5 x 5.2 x 1.3 mm (max.)
Mounting	Through Hole	SMT
Holder Type	HC-49/U	
Suggested Suppliers		
	KDS America	KDS America
	Toyocom U.S.A., Inc.	Hy-Q International (USA), Inc.
	Hy-Q International (USA), Inc.	Vectron Technologies, Inc.
	Vectron Technologies, Inc.	

Notes

1. Characteristics @ 25°C unless otherwise noted.
2. Supplier Information:

KDS America
Fountain Valley, CA
(714) 557-7833

Toyocom U.S.A., Inc.
Costa Mesa, CA
(714) 668-9081

Hy-Q International (USA), Inc.
Enlanger, KY
(606) 283-5000

Vectron Technologies, Inc.
Lowell, NH
(603) 598-0074

5.3 SCHEMATICS

A typical application schematic for the modem with serial DTE interface packaged in a 68-pin PLCC is shown in Figure 5-1.

A typical interface schematic for the modem with parallel host interface packaged in a 68-pin is shown in Figure 5-2.

Consult AccelerATor Kits or reference designs for full schematics of typical applications. A complete schematic for a parallel host application is supplied with the RCV144ACF/SP AccelerATor Kit (AK28-D430) and the RCV336ACF/SP AccelerATor Kit (AK28-D470).

5.4 OTHER CONSIDERATIONS

The DAA design described in this designer's guide is a wet DAA, i.e., it requires line current to be present to pass the signal. Therefore, if the modem is to be connected back-to-back by cable directly to another modem, the modems will not be able to connect. The DAAs must be modified to operate dry, i.e., without line current, when used in this environment.

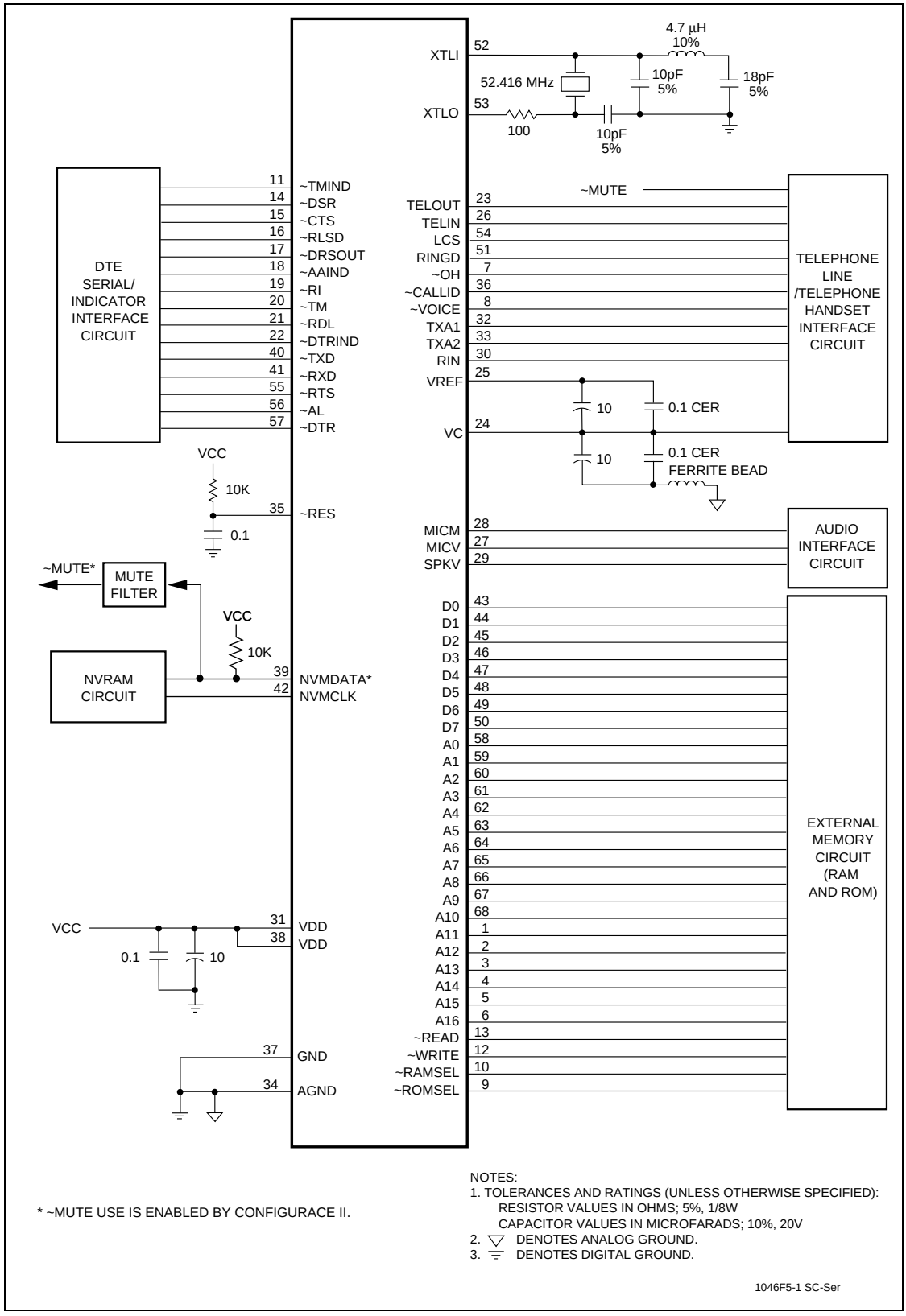

Figure 5-1. Interface Schematic - Modem with Serial DTE Interface - 68-Pin PLCC

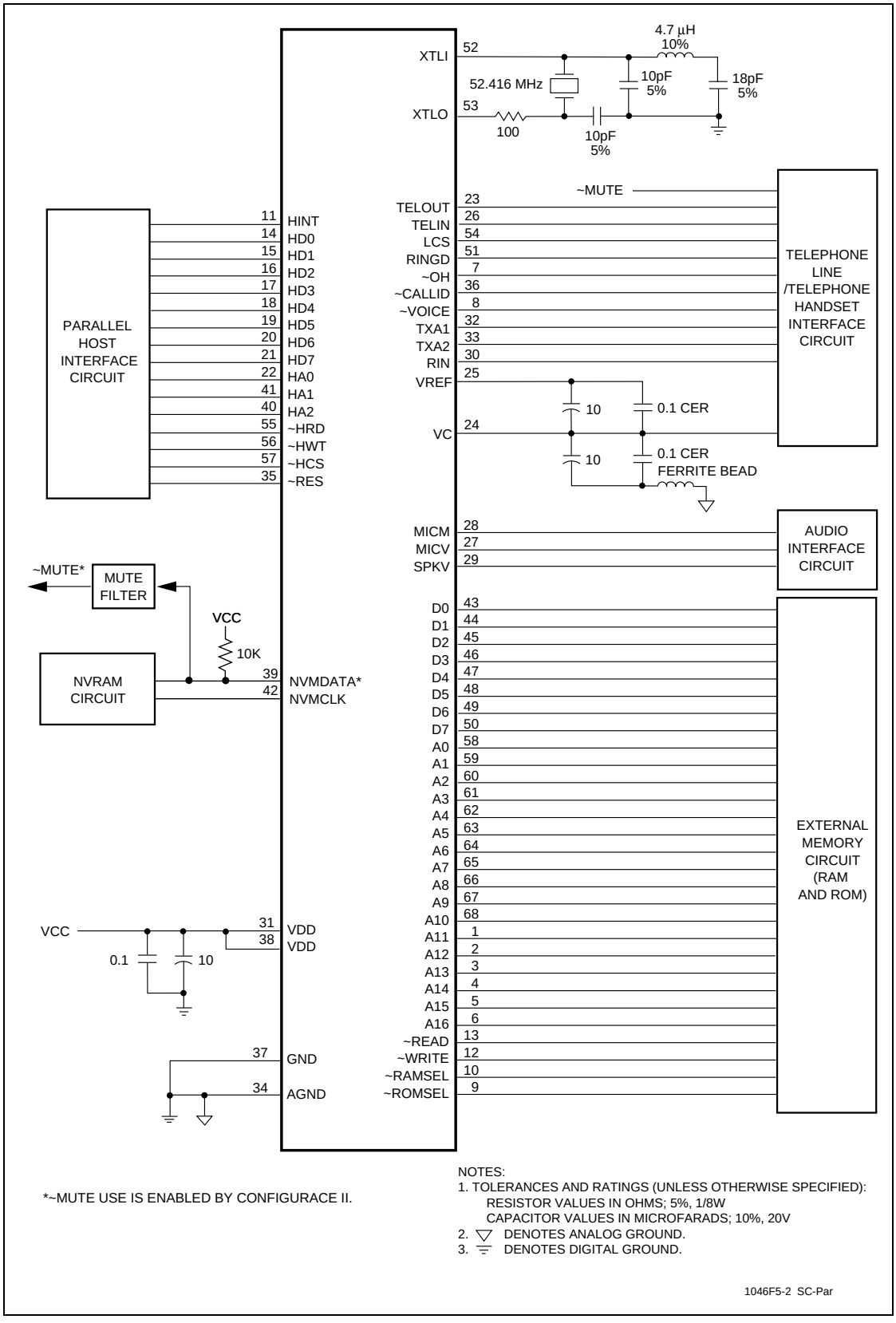

Figure 5-2. Interface Schematic - Modem with Parallel Host Interface - 68-Pin PLCC

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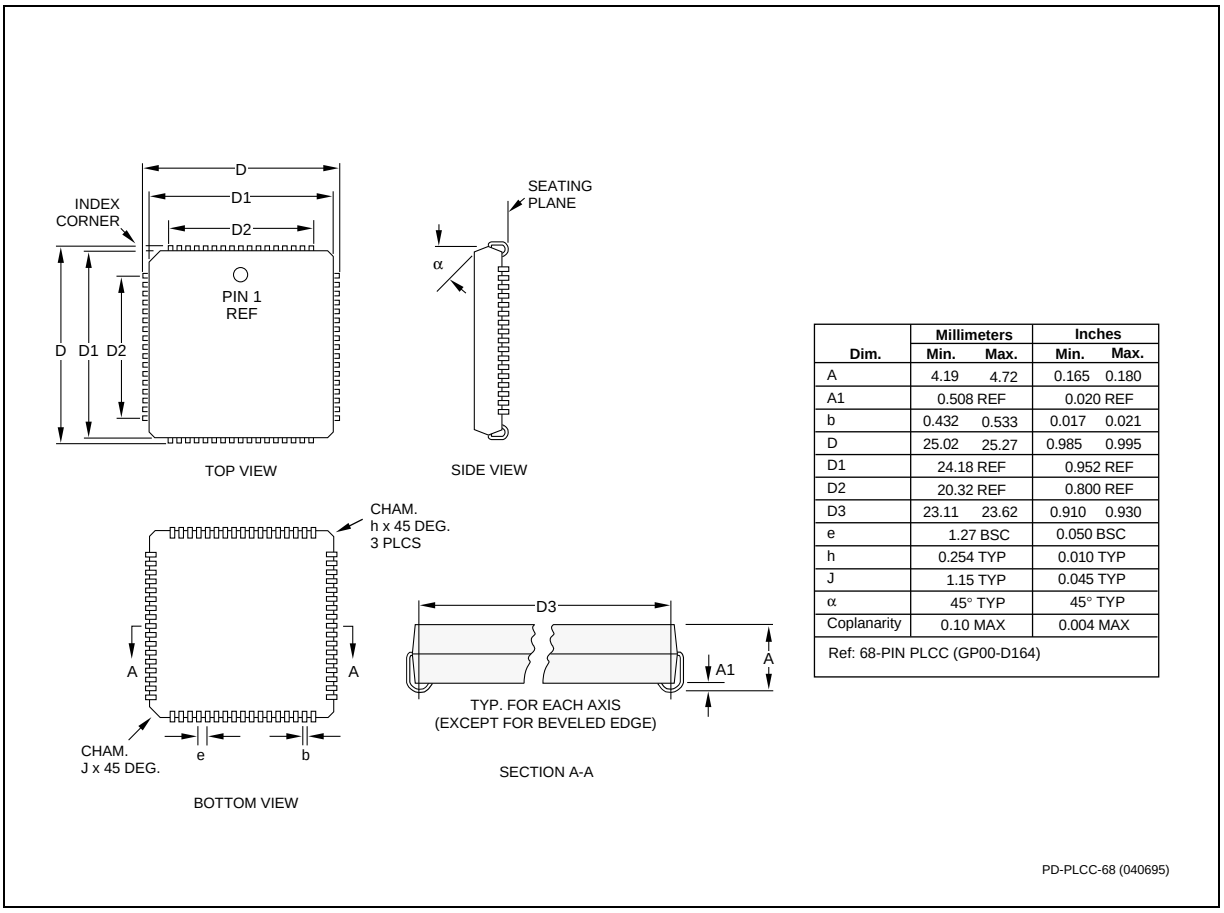
6. PACKAGE DIMENSIONS

The package dimensions are shown in Figure 6-1 (68-pin PLCC).



Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	4.19	4.72	0.165	0.180
A1	0.508 REF		0.020 REF	
b	0.432	0.533	0.017	0.021
D	25.02	25.27	0.985	0.995
D1	24.18 REF		0.952 REF	
D2	20.32 REF		0.800 REF	
D3	23.11	23.62	0.910	0.930
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
Coplanarity	0.10 MAX		0.004 MAX	
Ref: 68-PIN PLCC (GP00-D164)				

Figure 6-1. Package Dimensions - 68-Pin PLCC

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7. AT COMMANDS

7.1 BASIC AT COMMANDS

A/	Re-execute command.
A	Go off-hook and attempt to answer a call.
B0	Select V.22 connection at 1200 bps.
B1	Select Bell 212A connection at 1200 bps.
C1	Return OK message.
Dn	Dial modifier.
E0	Turn off command echo.
E1	Turn on command echo.
H0	Initiate a hang-up sequence.
H1	If on-hook, go off-hook and enter command mode.
I0	Report product code.
I1	Compute and report checksum.
I2	Compute checksum and report result of comparison to pressured checksum.
I3	Report firmware revision, model, and interface type.
I4	Report response programmed by an OEM.
I5	Report the country code parameter.
I6	Report modem data pump model and code revision.
I7	Reports the DAA code (world-class models only).
L0	Set low speaker volume.
L1	Set low speaker volume.
L2	Set medium speaker volume.
L3	Set high speaker volume.
M0	Turn speaker off.
M1	Turn speaker on during handshaking and turn speaker off while receiving carrier.
M2	Turn speaker on during handshaking and while receiving carrier.
M3	Turn speaker off during dialing and receiving carrier and turn speaker on during answering.
N0	Turn off automode detection.
N1	Turn on automode detection.
O0	Go on-line.
O1	Go on-line and initiate a retrain sequence.
P	Force pulse dialing.
Q0	Allow result codes to DTE.
Q1	Inhibit result codes to DTE.
Sn	Select S-Register as default.
Sn?	Return the value of S-Register n.
=v	Set default S-Register to value v.
?	Return the value of default S-Register.
T	Force DTMF dialing.
V0	Report short form (terse) result codes.
V1	Report long form (verbose) result codes.
W0	Report DTE speed in EC mode.
W1	Report line speed, EC protocol and DTE speed.
W2	Report DCE speed in EC mode.

X0	Report basic call progress result codes, i.e., OK, CONNECT, RING, NO CARRIER (also, for busy, if enabled, and dial tone not detected), NO ANSWER and ERROR.
X1	Report basic call progress result codes and connections speeds (OK, CONNECT, RING, NO CARRIER (also, for busy, if enabled, and dial tone not detected), NO ANSWER, CONNECT XXXX, and ERROR.
X2	Report basic call progress result codes and connections speeds, i.e., OK, CONNECT, RING, NO CARRIER (also, for busy, if enabled, and dial tone not detected), NO ANSWER, CONNECT XXXX, and ERROR.
X3	Report basic call progress result codes and connection rate, i.e., OK, CONNECT, RING, NO CARRIER, NO ANSWER, CONNECT XXXX, BUSY, and ERROR.
X4	Report all call progress result codes and connection rate, i.e., OK, CONNECT, RING, NO CARRIER, NO ANSWER, CONNECT XXXX, BUSY, NO DIAL TONE and ERROR.
Y0	Disable long space disconnect before on-hook.
Y1	Enable long space disconnect before on-hook.
Z0	Restore stored profile 0 after warm reset.
Z1	Restore stored profile 1 after warm reset.

&C0	Force RLSD active regardless of the carrier state.	
&C1	Allow RLSD to follow the carrier state.	
&D0	Interpret DTR ON-to-OFF transition per &Qn:	
	&Q0, &Q5, &Q6	The modem ignores DTR.
	&Q1, &Q4	The modem hangs up.
	&Q2, &Q3	The modem hangs up.
&D1	Interpret DTR ON-to-OFF transition per &Qn:	
	&Q0, &Q1, &Q4, &Q5, &Q6	Asynchronous escape.
	&Q2, &Q3	The modem hangs up.
&D2	Interpret DTR ON-to-OFF transition per &Qn:	
	&Q0 thru &Q6	The modem hangs up.
&D3	Interpret DTR ON-to-OFF transition per &Qn:.	
	&Q0, &Q1, &Q4, &Q5, &Q6	The modem performs soft reset.
	&Q2, &Q3	The modem hangs up.
&F0	Restore factory configuration 0.	
&F1	Restore factory configuration 1.	
&G0	Disable guard tone.	
&G1	Disable guard tone.	
&G2	Enable 1800 Hz guard tone.	
&J0	Set S-Register response only for compatibility.	
&J1	Set S-Register response only for compatibility.	
&K0	Disable DTE/DCE flow control.	
&K3	Enable RTS/CTS DTE/DCE flow control.	
&K4	Enable XON/XOFF DTE/DCE flow control.	
&K5	Enable transparent XON/XOFF flow control.	
&K6	Enable both RTS/CTS and XON/XOFF flow control.	
&L0	Select dial up line operation.	
&M0	Select direct asynchronous mode.	
&P0	Set 10 pps pulse dial with 39%/61% make/break.	
&P1	Set 10 pps pulse dial with 33%/67% make/break.	
&P2	Set 20 pps pulse dial with 39%/61% make/break.	
&P3	Set 20 pps pulse dial with 33%/67% make/break.	
&Q0	Select direct asynchronous mode.	
&Q4	Select Hayes AutoSync mode.	
&Q5	Modem negotiates an error corrected link.	
&Q6	Select asynchronous operation in normal mode.	
&R0	CTS tracks RTS (async) or acts per V.25 (sync).	
&R1	CTS is always active.	

&S0	DSR is always active.
&S1	DSR acts per V.25.
&T0	Terminate any test in progress.
&T1	Initiate local analog loopback.
&T2	Returns ERROR result code.
&T3	Initiate local digital loopback.
&T4	Allow remote digital loopback.
&T5	Disallow remote digital loopback request.
&T6	Request an RDL without self-test.
&T7	Request an RDL with self-test.
&T8	Initiate local analog loop with self-test.
&V	Display current configurations.
&W0	Store the active profile in NVRAM profile 0.
&W1	Store the active profile in NVRAM profile 1.
&Y0	Recall stored profile 0 upon power up.
&Y1	Recall stored profile 1 upon power up.
&Zn=x	Store dial string x (to 34) to location n (0 to 3).
%E0	Disable line quality monitor and auto retrain.
%E1	Enable line quality monitor and auto retrain.
%E2	Enable line quality monitor and fallback/fall forward.
%L	Return received line signal level.
%Q	Report the line signal quality.
%TTn	PTT certification test signals.
\Kn	Controls break handling during three states:
When modem receives a break from the DTE:	
\K0,2,4	Enter on-line command mode, no break sent to the remote modem.
\K1	Clear buffers and send break to remote modem.
\K3	Send break to remote modem immediately.
\K5	Send break to remote modem in sequence with transmitted data.
When modem receives \B in on-line command state:	
\K0,1	Clear buffers and send break to remote modem.
\K2,3	Send break to remote modem immediately.
\K4,5	Send break to remote modem in sequence with transmitted data.
When modem receives break from the remote modem:	
\K0,1	Clear data buffers and send break to DTE.
\K2,3	Send a break immediately to DTE.
\K4,5	Send a break with received data to the DTE.
\N0	Select normal speed buffered mode.
\N2	Select reliable link mode.
\N3	Select auto reliable mode.
\N4	Force LAPM mode.
\N5	Force MNP mode.
\V0	Disable single line connect message.
\V1	Enable single line connect message.
+MS	Select modulation
**0	Download to flash memory at last sensed speed.
**1	Download to flash memory at 38.4 kbps.
**2	Download to flash memory at 57.6 kbps.

-SDR=0	Disable Distinctive Ring.
-SDR=1	Enable Distinctive Ring Type 1.
-SDR=2	Enable Distinctive Ring Type 2.
-SDR=3	Enable Distinctive Ring Type 1 and 2.
-SDR=4	Enable Distinctive Ring Type 3.
-SDR=5	Enable Distinctive Ring Type 1 and 3.
-SDR=6	Enable Distinctive Ring Type 2 and 3.
-SDR=7	Enable Distinctive Ring Type 1, 2, and 3.

7.2 ECC COMMANDS

%C0	Disable data compression.
%C1	Enable MNP 5 data compression.
%C2	Enable V.42 bis data compression.
%C3	Enable both V.42 bis and MNP 5 compression.
\A0	Set maximum block size in MNP to 64.
\A1	Set maximum block size in MNP to 128.
\A2	Set maximum block size in MNP to 192.
\A3	Set maximum block size in MNP to 256.
\Bn	Send break of n x 100 ms.

7.3 MNP 10 COMMANDS

-K0	Disable MNP 10 extended services.
-K1	Enable MNP 10 extended services.
-K2	Enable MNP 10 extended services detection only.
-SEC=0	Disable MNP 10EC.
-SEC=1,[<tx level>]	Enable MNP 10EC and set transmit level <tx level> 0 to 30 (0 dBm to -30 dBm).

7.4 W-CLASS COMMANDS

*B	Display list of permanently blacklisted numbers.
*D	Display list of delayed numbers.
*NCnn	Change country to one of eight in NVRAM.

7.5 CALLER ID COMMANDS

#CID=0	Disable Caller ID.
#CID=1	Enable Caller ID with formatted presentation.
#CID=2	Enable Caller ID with unformatted presentation.

7.6 FAX CLASS 1 COMMANDS

+FCLASS=n	Service class.
+FAE=n	Data/fax auto answer
+FRH=n	Receive data with HDLC framing.
+FRM=n	Receive data.
+FRS=n	Receive silence.
+FTH=n	Transmit data with HDLC framing.
+FTM=n	Transmit data.
+FTS=n	Stop transmission and wait.

7.7 VOICE COMMANDS

#BDR	Select baud rate (turn off autobaud).
#CLS	Select data, fax, or voice.
#MDL?	Identify model.
#MFR?	Identify manufacturer.
#REV?	Identify revision level.
#TL	Audio output transmit level.
#VBQ?	Query buffer size.
#VBS	Bits per sample.
#VBT	Beep tone timer.
#VCI?	Identify compression method.
#VGT	Set playback volume in the command state.
#VLS	Voice line select.
#VRA	Ringback goes away timer (originate).
#VRN	Ringback never came timer (originate).
#VRX	Voice receive mode.
#VSD	Enable silence deletion (no function; command response only).
#VSK	Buffer skid setting.
#VSP	Silence detection period (voice receive).
#VSR	Sampling rate selection.
#VSS	Silence detection tuner (voice receive).
#VTD	DTMF/tone reporting.
#VTM	Enable timing mark placement.
#VTS	Generate tone signals.
#VTX	Voice transmit mode.

7.8 VOICEVIEW COMMANDS

+FCLASS=n	Service class
-SVV	Originate VoiceView data mode
-SAC	Accept data mode request
-SIP	Initialize VoiceView parameters
-SIC	Reset capabilities data to default setting
-SSQ	Initiate capabilities query
-SDA	Originate modem data mode
-SFX	Originate FAX data mode
-SMT	Mute telephone
-SDS	Disable switchhook status monitoring
-SQR	Capabilities query response control
-SCD	Capabilities data
-SER?	Error status (read only)
-DTP	VoiceView transmission speed
-SSR	Start sequence response control
+FLO	Flow control select
+FPR	Serial port rate control
-SSV	VoiceView data mode start sequence event
-SFA	Facsimile data node start sequence event
-SMD	Modem data mode start sequence event
-SRA	Receive ADSI response event
-SRQ	Receive capabilities query event
-SRC:	Receive capabilities information event
-STO	Talk-off event

7.9 AUDIOSPAN COMMANDS

-SMC=x	Enable/disable ML144 data burst
-SMS=x,y,z,t	Select AudioSpan/DSVD mode
-SQS=x,y	Select AudioSpan modulation

* Serial interface operation only.

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