R288F V.34 Fax/V.17 Fax Modem

Designer's Guide (Preliminary)

Rockwell International
Digital Communications Division

Order No. 1069
Rev. 1, December 19, 1996

NOTICE

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1. INTRODUCTION

1.1 SUMMARY

The Rockwell R288F modem is a V.34 half-duplex modem that supports Group 3 facsimile send and receive speeds up to 33600 bps using the V.34 half-duplex mode. Using a V.34 technique to optimize modem configuration for line conditions, the modem connects at the highest data rate that the channel can support from 33600 bps to 2400 bps.

The modem can operate over the public switched telephone network (PSTN) through the appropriate line terminator provided by a data access arrangement (DAA).

The modem satisfies the requirements specified in ITU-T recommendations V.34, V.17, V.29, V.27 ter, V.23, V.21, and meets the binary signaling requirements of V.8 and T.30.

Internal HDLC support eliminates the need for an external serial input/output (SIO) device in the DTE for products incorporating error correction and T.30 protocol. The modem can perform HDLC framing per T.30 at all data speeds. CRC generation/checking along with zero insertion/deletion enhances SDLC/HDLC frame operations.

An FSK flag pattern detector facilitates FSK detection during high speed reception.

The modem features a programmable DTMF transmitter/receiver and three programmable tone detectors which can operate in the tone mode.

The modem offers lower power consumption and small size to allow the design of compact system enclosures for use in industrial, office, and home environment.

The modem is available in a 68-pin PLCC package.

1.2 FEATURES

- 2-wire half-duplex fax modem modes with send and receive rates up to 33600 bps.
  - V.34, V.17, V.29, V.27 ter, and V.21 channel 2
  - Short train option in V.17 and V.27 ter
- 2-wire full-duplex data modem modes
  - V.21, V.23 (75 bps TX/1200 bps RX or 1200 bps TX/ 75 bps RX)
- PSTN session starting
  - V.8 signaling
- HDLC support at all speeds
  - Flag generation, 0 bit stuffing, ITU CRC-16 or CRC-32 calculation and generation
  - Flag detection, 0 bit deletion, ITU CRC-16 or CRC-32 check sum error detection
  - FSK flag pattern detection during high speed receiving
- Tone modes and features
  - Programmable single or dual tone generation
  - DTMF receive
  - Tone detection with three programmable tone detectors
- Serial synchronous data
- Parallel synchronous data
- Automatic rate adaptation (ARA)
- TTL and CMOS compatible DTE interface
  - ITU-T V.24 (EIA/TIA-232-E) (data/control)
  - Microprocessor bus (data/configuration/control)
- Receive dynamic range: –9 dBm to –43 dBm (For non-V.34 modes, may be set to: 0 to -43 dBm.)
- Programmable turn-on and turn-off thresholds
- Programmable transmit level: 0 to -15 dBm
- Adjustable speaker output to monitor received signal
- DMA support interrupt lines
- Two 16-byte FIFO data buffers for burst data transfer
- NRZI encoding/decoding
- 511 pattern generation/detection
- Diagnostic capability
- +5V operation
- Typical power consumption:
  - Normal mode: 700 mW
  - Sleep mode: 65 mW
- 68-pin PLCC package

1.3 TECHNICAL DESCRIPTION

Configurations and Rates

The selectable modem configurations, signaling rates, and data rates are listed in Table 1-1.

Automatic Rate Adaptation (ARA)

In V.34 mode, automatic rate adaptation (ARA) can be enabled to select the highest data rate possible based on the measured eye quality monitor (EQM). This selection occurs during handshake.

Tone Generation

The modem can generate single or dual voice-band tones from 0 Hz to 3600 Hz with a resolution of 0.15 Hz and an accuracy of ± 0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the modem to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to ITU-T recommendations V.34, V.17, V.33, V.29, V.27 ter, V.23, or V.21, depending on the configuration.

Transmitted Data Spectrum

The transmitter spectrum is shaped by raised cosine filter functions as follows:

Configuration	Raised Cosine Filter Function
V.34	Square root of 12.5%
V.27 ter, V.17, V.33, V.29	Square root of 20%

RTS – CTS Response Time

The response times of CTS relative to a corresponding transition of RTS are listed in Table 1-2.

Transmit Level

The transmitter output level is selectable from 0 dBm to –15 dBm in 1 dB steps and is accurate to ±0.5 dB when used with an external hybrid. The output level can also be fine tuned by changing a gain constant in modem DSP RAM.

Note: In V.34 mode, the transmit level may be automatically changed during the handshake. This automatic adjustment of the transmit level may be disabled via a parameter in DSP RAM.

Scrambler/Descrambler

A self-synchronizing scrambler/descrambler is used in accordance with the selected configuration.

Answer Tone

In V.8, V.23, and V.21, the modem generates a 2100 Hz answer tone at the beginning of the answer handshake when the NV25 bit is a zero. The answer tone, if generated in V.8 mode, has 180° phase reversals every 0.45 second to disable network echo cancellers. The duration of the answer tone must be controlled by the host.

Receive Level

The modem satisfies performance requirements for received line signal levels from –9 dBm to –43 dBm measured at the Receiver Analog (RXA) (TIP and RING) input. The receive level can be increased up to 0 dBm in V.17, V.29 and V.27ter modes by using the procedure described in Section 4.13.

Table 1-1. Configurations, Signaling Rates, and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Symbol Rate (Symbols/Sec.)	Bits/Symbol - Data	Bits/Symbol - TCM	Constellation Points
V.34 33600 TCM	TCM	Note 2	33600	3429 only	Note 2	Note 2	Note 2
V.34 31200 TCM	TCM	Note 2	31200	Note 2	Note 2	Note 2	Note 2
V.34 28800 TCM	TCM	Note 2	28800	Note 2	Note 2	Note 2	Note 2
V.34 26400 TCM	TCM	Note 2	26400	Note 2	Note 2	Note 2	Note 2
V.34 24000 TCM	TCM	Note 2	24000	Note 2	Note 2	Note 2	Note 2
V.34 21600 TCM	TCM	Note 2	21600	Note 2	Note 2	Note 2	Note 2
V.34 19200 TCM	TCM	Note 2	19200	Note 2	Note 2	Note 2	Note 2
V.34 16800 TCM	TCM	Note 2	16800	Note 2	Note 2	Note 2	Note 2
V.34 14400 TCM	TCM	Note 2	14400	Note 2	Note 2	Note 2	Note 2
V.34 12000 TCM	TCM	Note 2	12000	Note 2	Note 2	Note 2	Note 2
V.34 9600 TCM	TCM	Note 2	9600	Note 2	Note 2	Note 2	Note 2
V.34 7200 TCM	TCM	Note 2	7200	Note 2	Note 2	Note 2	Note 2
V.34 4800 TCM	TCM	Note 2	4800	Note 2	Note 2	Note 2	Note 2
V.34 2400 TCM	TCM	Note 2	2400	Note 2	Note 2	Note 2	Note 2
V.23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
V.17 14400 TCM	TCM	1800	14400	2400	6	1	128
V.17 12000 TCM	TCM	1800	12000	2400	5	1	64
V.17 9600 TCM	TCM	1800	9600	2400	4	1	32
V.17 7200 TCM	TCM	1800	7200	2400	3	1	16
V.29 9600	QAM	1700	9600	2400	4	0	16
V.29 7200	QAM	1700	7200	2400	3	0	8
V.29 4800	QAM	1700	4800	2400	2	0	4
V.27 4800	DPSK	1800	4800	1600	3	0	8
V.27 2400	DPSK	1800	2400	1200	2	0	4
V.21 Channel 2	FSK	1750	300	300	1	0	–

Notes:

1. Modulation legend: TCM: Trellis-Coded Modulation; QAM: Quadrature Amplitude Modulation; FSK: Frequency Shift Keying; DPSK: Differential Phase Shift Keying

2. Adaptive; established during handshake:

	Carrier Frequency (Hz)	
Symbol Rate (Baud)	**V.34 Low Carrier**	**V.34 High Carrier**
2400	1600	1800
2800	1680	1867
3000	1800	2000
3200	1829	1920
3429	1959	1959

Table 1-2. RTS-CTS Response Times

Configuration	RTS-CTS Response[1]	Turn-Off Sequence[3]
V.33/V.17 Long	1393 ms[2]	15 ms[4]
V.33/V.17 Short	142 ms[2]	15 ms[4]
V.29	253 ms[2]	12 ms[4]
V.27 4800 Long	708 ms[2]	7 ms[4]
V.27 4800 Short	50 ms[2]	7 ms[4]
V.27 2400 Long	943 ms[2]	10 ms[4]
V.27 2400 Short	67 ms[2]	10 ms[4]
V.21	500 ms	N/A
V.23	210 ms	N/A

Notes:

1. Times listed are CTS turn-on. The CTS OFF-to-ON response time is host programmable in DSP RAM.
2. Add echo protector tone duration plus 20 ms when echo protector tone is used during turn-on.
3. Turn-off sequence consists of transmission of remaining data and scrambled ones. CTS turn-off is less than 2 ms for all configurations.
4. Plus 20 ms of no transmitted energy.
5. N/A = not applicable.

Receiver Timing

The timing recovery circuit can track a frequency error in the associated transmit timing source of ±0.01%.

Carrier Recovery

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector (~RLSD) is off. ~RLSD can be clamped off (RLSDE bit).

Data Formats

Serial Synchronous Data (Except control channel mode, see below.)

Data rate: 33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps ±0.01%.

Clock: Internal

Note: In control channel mode, only the parallel data mode is supported.

Parallel Synchronous Data

Normal sync: 8-bit data for transmit and receive

Data rate: 33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps ±0.01%.

SDLC/HDLC support

Transmitter: Flag generation, 0 bit stuffing, ITU-T CRC-16 or CRC-32 generation.

Receiver: Flag detection, 0 bit deletion, ITU-T CRC-16 or CRC-32 checking.

Auto-Dialing and Auto-Answering Control

The host can perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection, and a comprehensive supervisory tone detection scheme. The major parameters are host programmable.

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path.

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This circuit is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The squarer may be disabled by the SQDIS bit causing tone detector C to be an eighth order filter. The tone detectors are disabled in data mode.

The tone detection sample rate is 9600 Hz in V.8 and V.34 modes and is 7200 Hz in non-V.34 modes. The default call progress filter coefficients are based on a 7200 Hz sampling rate and apply to non-V.34 modes only. The maximum detection bandwidth is equal to one-half the sample rate.

Supervisory Tone Detectors, Default Characteristics

The default bandwidths and thresholds of the tone detectors are as follows:

Tone Detector	Bandwidth	Turn-On Threshold	Turn-Off Threshold
A	245 – 650 Hz	–25 dBm	–31 dBm
B	360 – 440 Hz	–25 dBm	–31 dBm
Prefilter	0 – 500 Hz	N/A	N/A
C*	50 – 110 Hz	-26 dBm	-26 dBm
* Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range –1 dBm to –26 dBm.			

511 Pattern Generation/Detection

In a synchronous mode, a 511 pattern can be generated and detected (control bit S511). Use of this bit pattern during self-test eliminates the need for external test equipment.

Transmit and Receive FIFO Data Buffers

Two 16-byte first-in first-out (FIFO) data buffers allow the DTE/host to rapidly output up to 16 bytes of transmit data and input up to 16 bytes of accumulated received data. The receiver FIFO is always enabled. The transmitter FIFO is enabled by the FIFOEN control bit. TXHF and RXHF bits indicate the corresponding FIFO buffer half full (8 or more bytes loaded) status. TXFNF and RXFNE bits indicate the TX FIFO buffer not full and RX FIFO buffer not empty status, respectively. An interrupt mask register allows an interrupt request to be generated whenever the TXFNF, RXFNE, RXHF, or TXHF status bit changes state. (See Section 4.4, Function 74.)

DMA Support Interrupt Request Lines

DMA support is available in synchronous data modes. Control bit DMAE enables and disables DMA support. When DMA support is enabled, the modem ~RI and ~DSR lines are assigned to Transmitter Request (TXRQ) and Receiver Request (RXRQ) hardware output interrupt request lines, respectively. The TXRQ and RXRQ signals follow the assertion of the TDBE and RDBF interrupt bits thus allowing the DTE/host to respond immediately to the interrupt request without masking out status bits to determine the interrupt source.

NRZI Encoding/Decoding

NRZI data encoding/decoding may be selected in synchronous modes instead of the default NRZ (control bit NRZIEN). In NRZ encoding, a 1 is represented by a high level and a 0 is represented by a low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

ITU-T CRC-32 Support

ITU-T CRC-32 generation/checking may be selected instead of the default ITU-T CRC-16 in HDLC mode using DSP RAM access.

Caller ID Demodulation

Caller ID information can be demodulated in V.23 1200 receive configuration and presented to the host/DTE in serial (RXD) and parallel (RBUFFER) form.

Relay Control. Direct control of the off-hook and talk/data relays is provided. Internal relay drivers allow direct connection to the off-hook and talk/data relays. The talk/data relay output can optionally be used for pulse dial.

Speaker Interface

A SPKR output is provided with on/off and volume control logic incorporated in the modem, requiring only an external amplifier to drive a loudspeaker.

2. HARDWARE INTERFACE

2.1 HARDWARE INTERFACE SIGNALS

The functional interconnect diagram (Figure 2-1) shows the typical modem connection in a system. In this diagram, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). An active low signal is indicated by a tilde preceding the signal name (e.g., ~RESET).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., ~RDCLK), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The pin assignments for the modem packaged in a single 68-pin PLCC are shown in Figure 2-2 and are listed in Table 2-1.

The hardware interface signals are described in Table 2-2.

The digital interface characteristics are defined in Table 2-3.

The analog interface characteristics are defined in Table 2-4.

The power requirements are defined in Table 2-5.

The absolute maximum ratings are listed in Table 2-6.

The timing for DTE host microprocessor interface bus waveforms is shown in Table 2-7. The host bus waveforms are illustrated in Figure 2-3.

The DTE serial interface waveforms are illustrated in Figure 2-4.

Eye pattern diagnostic waveforms are illustrated in Figure 2-5.

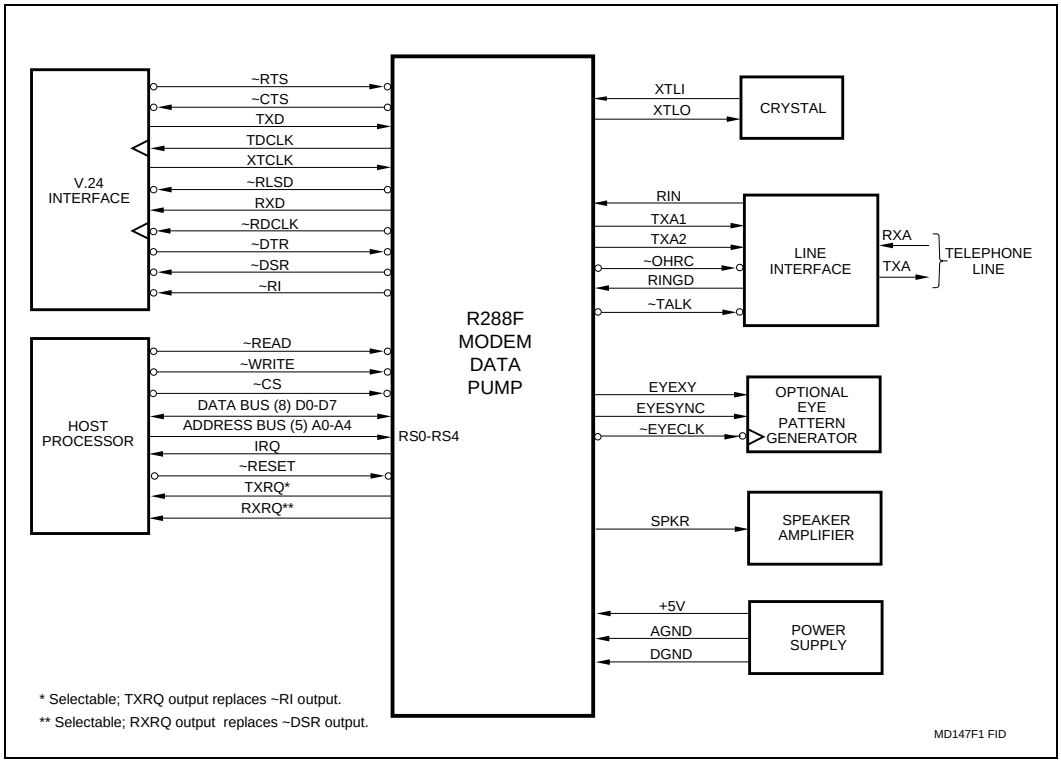


Figure 2-1. Modem Functional Interface Signals

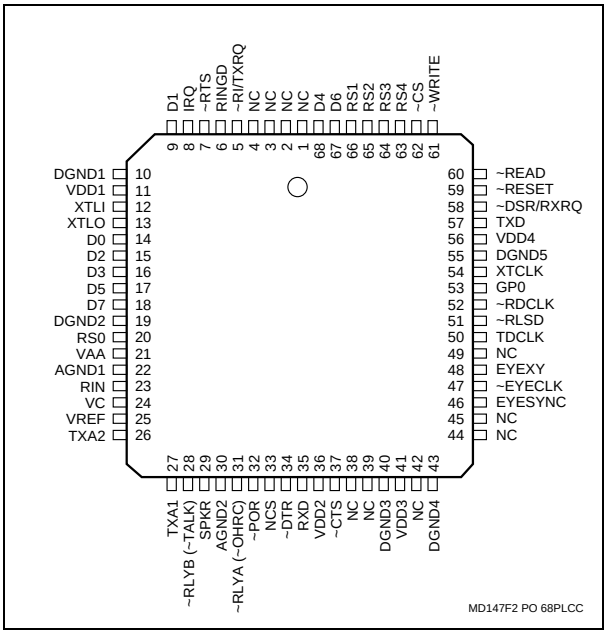


Figure 2-2. MDP Pin Signals - 68-Pin PLCC

Table 2-1. MDP Pin Signals - 68-Pin PLCC

Pin	Signal Label	I/O Type	Interface[3]	Pin	Signal Label	I/O Type	Interface
1	NC		NC	35	RXD	OA	DTE Serial Interface
2	NC	-	-	36	VDD2	PWR	
3	NC	-	-	37	~CTS	OA	DTE Serial Interface
4	NC	-	-	38	NC	-	-
5	~RI/TXRQ	OA	DTE Serial/DMA Interface	39	NC	-	-
6	RINGD	IA	LIU: RINGD	40	DGND3	GND	-
7	~RTS	IA	DTE Serial Interface	41	VDD3	PWR	-
8	IRQ	OA	Host Parallel Interface	42	NC	-	-
9	D1	IA/OB	Host Parallel Interface	43	DGND4	GND	-
10	DGND1	GND		44	NC	-	-
11	VDD1	PWR		45	NC	-	-
12	XTLI	I	Crystal/Clock Circuit	46	EYESYNC	OA	Eye Pattern Test Circuit
13	XTLO	O	Crystal/Clock Circuit	47	~EYECLK	OA	Eye Pattern Test Circuit
14	D0	IA/OB	Host Parallel Interface	48	EYEXY	OA	Eye Pattern Test Circuit
15	D2	IA/OB	Host Parallel Interface	49	NC	-	-
16	D3	IA/OB	Host Parallel Interface	50	TDCLK	OA	DTE Serial Interface
17	D5	IA/OB	Host Parallel Interface	51	~RLSD	OA	DTE Serial Interface
18	D7	IA/OB	Host Parallel Interface	52	~RDCLK	OA	DTE Serial Interface
19	DGND2	GND		53	GP0	MI	MDP: EYESYNC
20	RS0	IA	Host Parallel Interface	54	XTCLK	IA	DTE Serial Interface
21	5VA	PWR		55	DGND5	GND	
22	AGND1	GND		56	VDD4	PWR	
23	RIN	I(DA)	Line Interface	57	TXD	IA	DTE Serial Interface
24	VC	MI	To GND through capacitors	58	~DSR/RXRQ	OA	DTE Serial/DMA Interface
25	VREF	MI	To VC through capacitors	59	~RESET	OA	Host Parallel Interface
26	TXA2	O(DD)	Line Interface	60	~READ	IA	Host Parallel Interface
27	TXA1	O(DD)	Line Interface	61	~WRITE	IA	Host Parallel Interface
28	~TALK (~RLYB)	OA	Line Interface	62	~CS	IA	Host Parallel Interface
29	SPKR	O(DF)	Speaker Circuit	63	RS4	IA	Host Parallel Interface
30	AGND2	GND		64	RS3	IA	Host Parallel Interface
31	~OHRC (~RLYA)	OD	Line Interface	65	RS2	IA	Host Parallel Interface
32	~POR	MI	MDP: ~RESET	66	RS1	IA	Host Parallel Interface
33	NC	-	-	67	D6	IA/OB	Host Parallel Interface
34	~DTR	IA	DTE Serial Interface	68	D4	IA/OB	Host Parallel Interface

Notes:

1. I/O types:
   - MI = Modem interconnect.
   - IA, IB = Digital input.
   - OA, OB = Digital output.
   - I(DA) = Analog input.
   - O(DD), O(DF) = Analog output.
2. NC = No external connection allowed.
3. Interface Legend:
   - MDP = Modem Data Pump
   - DTE = Data Terminal Equipment

Table 2-2. MDP Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI, XTLO	I, O	**Crystal In and Crystal Out.** Connect the MDP to an external crystal circuit consisting of a 52.146 MHz crystal, three capacitors, and an inductor.
~RESET	IA	**Reset.** ~RESET low holds the modem in the reset state. ~RESET going high releases the modem from the reset state and initiates normal operation using power turn-on (default) values. ~RESET must be held low for at least 3 µs. The modem is ready to use 400 ms after the low-to-high transition of ~RESET.
VDD	PWR	**+ 5V Digital Supply.** +5V± 5%.
+5VA	PWR	**+ 5V Analog Supply.** +5V± 5%.
DGND	GND	**Digital Ground.** Connect to ground.
AGND	GND	**Analog Ground.** Connect to ground.
		MCU INTERFACE
		Address, data, control, and interrupt hardware interface signals allow modem connection to an 8086-compatible microprocessor bus. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.
RS0–RS4	IA	**Register Select Lines.** The five active high register select lines (RS0–RS4) address interface memory registers within the modem interface memory. These lines are typically connected to the five least significant lines (A0–A4) of the address bus. The modem decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4, while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7, while the least significant data bit is D0.
~CS	IA	**Chip Select.** ~CS selects the modem for microprocessor bus operation. ~CS is typically generated by decoding host address bus lines.
~READ	IA	**Read Enable.** During a read cycle (~READ asserted), data from the selected interface memory register is gated onto the data bus by means of three-state drivers in the modem. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state.
~WRITE	IA	**Write Enable.** During a write cycle (~WRITE asserted), data from the data bus is copied into the selected modem interface memory register, with high and low bus levels representing one and zero bit states, respectively.
IRQ	OA	I**nterrupt Request.** The modem IRQ output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The IRQ output can be enabled in the modem interface memory to indicate immediate change of conditions. The use of IRQ is optional depending upon modem application. The IRQ output is driven by a TTL-compatible CMOS driver.
TXRQ	OA	**Transmitter Request.** When control bit DMAE in interface memory is set, this pin operates as the TXRQ output function rather than the ~RI function. TXRQ is a high active signal that follows the state of the TDBE bit. DMA operation is available in synchronous modes.
RXRQ	OA	**Receiver Request.** When control bit DMAE in interface memory is set, this pin operates as the RXRQ output function rather than the ~DSR function. RXRQ is a high active signal that follows the state of the RDBF bit. DMA operation is available in synchronous modes.

Table 2-2. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
DTE SERIAL INTERFACE		
		Timing, data, control, and status signals provide a V.24-compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within a printed circuit board, stand-alone modem enclosures, or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA/RS-232-D voltage levels.
TXD	IA	**Transmitted Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output.
~RTS	IA	**Request to Send.** Activating ~RTS causes the modem to transmit data on TXD when ~CTS becomes active. The ~RTS pin is logically ORed with the RTS bit.
~CTS	OA	**Clear To Send.** ~CTS active indicates to the local DTE that the modem will transmit any data present on TXD. CTS response times from an active condition of RTS are shown in Table 1-2.
~RLSD	OA	**Received Line Signal Detector.** ~RLSD active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than -43 dBm. The ~RLSD on and off thresholds are host programmable in DSP RAM.
~DTR	IA	**Data Terminal Ready.** In V.34 configuration, activating ~DTR initiates the handshake sequence, provided that the DATA bit is a 1. If in answer mode, the modem immediately sends answer tone. In V.21 or V.23 configuration, activating ~DTR causes the modem to enter the data state provided that the DATA bit is a 1. If in answer mode, the modem immediately sends answer tone. During the data mode, deactivating ~DTR causes the transmitter and receiver to turn off and return to the idle state. The ~DTR input and the DTR control bit are logically ORed.
~DSR	OA	**Data Set Ready.** ~DSR ON indicates that the modem is in the data transfer state. ~DSR OFF indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator (~RI). ~DSR is OFF when the modem is in a test mode (i.e., local analog or remote digital loopback). The DSR status bit reflects the state of the ~DSR output.
~RI	OA	**Ring Indicator.** ~RI output follows the ringing signal present on the line with a low level (0 V) during the ON time, and a high level (+5 V) during the OFF time coincident with the ringing signal. The RI status bit reflects the state of the ~RI output.
TDCLK	OA	**Transmit Data Clock.** The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50±1%. The TDCLK source can be internal, external (input on XTCLK), or slave (to ~RDCLK) as selected by TXCLK bits in interface memory.
XTCLK	IA	**External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the modem XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output.
~RDCLK	OA	**Receive Data Clock.** The modem outputs a synchronous Receive Data Clock (~RDCLK) for USRT timing. The ~RDCLK frequency is the data rate (±0.01%) with a duty cycle of 50±1%. The ~RDCLK low-to-high transitions coincide with the center of the received data bits.

Table 2-2. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
		TELEPHONE LINE INTERFACE
TXA1, TXA2	O(DF)	**Transmit Analog 1 and 2.** The TXA1 and TXA2 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load.
RIN	I(DA)	**Receive Analog.** RIN is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit.
RINGD	IA	**Ring Detect.** The RINGD input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving RINGD should be a 4N35 optoisolator or equivalent. The circuit driving RINGD should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. Detected ring signals are reflected on the ~RI output signal as well as the RI bit.
~RLYA (~OHRC, CALLID)	OD	**Relay A Control.** The ~RLYA open collector output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms (13.9 mA max. @ 5.0V) and a must-operate voltage no greater than 4.0 VDC. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYA is controlled by host setting/resetting of the RA bit. In a typical application, ~RLYA is connected to the normally open Off-Hook relay (~OHRC). In this case, ~RLYA active closes the relay to connect the modem to the telephone line. Alternatively, in a typical application, ~RLYA is connected to the normally open Caller ID relay (CALLID). When the modem detects a Calling Number Delivery (CND) message, the ~RLYA output is asserted to close the CALLID relay in order to AC couple the CND information to the modem RIN input (without closing the off-hook relay and allowing loop current flow which would indicate an off-hook condition).
~RLYB (~TALK)	OD	**Relay B Control.** The ~RLYB open collector output can directly drive a +5V reed relay coil with a minimum resistance of 360 ohms (13.9 mA max. @ 5.0V) and a must-operate voltage no greater than 4.0 VDC. A clamp diode, such as a 1N4148, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). ~RLYB is controlled by host setting/resetting of the RB bit. In a typical application, ~RLYB is connected to the normally closed Talk/Data relay (~TALK). In this case, ~RLYB active opens the relay to disconnect the handset from the telephone line.
		DIAGNOSTIC SIGNALS
		Three signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEXY	OA	**Serial Eye Pattern X/Y Output.** EYEXY is a serial output containing two 15-bit diagnostic words (EYEX and EYEY) for display on the oscilloscope X axis (EYEX) and Y axis (EYEY). EYEX is the first word clocked out; EYEY follows. Each word has 8-bits of significance. Each 15-bit data word is shifted out most significant bit first with the seven most significant bits set to zero. EYEXY is clocked by the rising edge of ~EYECLK. This serial digital data must be converted to parallel digital form by a serial-to-parallel converter, and then to analog form by two digital-to-analog (D/A) converters.
~EYECLK	OA	**Serial Eye Pattern Clock.** ~EYECLK is a 288 kHz output clock for use by the serial-to-parallel converters. The low-to-high transitions of ~RDCLK coincide with the low-to-high transitions of ~EYECLK. ~EYECLK, therefore, can be used as a receiver multiplexer clock.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters.
		SPEAKER INTERFACE
SPKR	O(DF)	**Speaker Analog Output.** The SPKR output reflects the received analog input signal. The SPKR on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the SPKR output is clamped to the voltage at the VC pin. The SPKR output can drive an impedance as low as 300 ohms. In a typical application, the SPKR output is an input to an external LM386 audio power amplifier.

Table 2-2. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
REFERENCE SIGNALS AND MODEM INTERCONNECT		
VC	MI	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel.
VREF	MI	**High Voltage Reference.** Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
~POR	MI	**Power-On-Reset**. Connect to ~RESET.
DSP_RESET	MI	**DSP Reset.** Connect to ~RES.
RES	MI	**Reset.** Connect to DSP_RESET.
DSP_IRQ	MI	**DSP Interrupt Request.** Connect to ~IRQ.
~IRQ	MI	**Interrupt Request.** Connect to DSP_IRQ.
IA_CLKIN	MI	**IA Clock.** Connect to CLKIN.
CLKIN	MI	**Clock.** Connect to IA_CLKIN.
RMODE	MI	**Receiver Mode.** Connect to TMODE.
TMODE	MI	**Transmitter Mode.** Connect to RMODE.

Table 2-3. Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				Vdc	
Type IA and IB		2.0	–	V_{CC}		
Type ID		0.8 V_{CC}	–	V_{CC}		
Input High Current	I_{IH}	–	–	40	µA	
Input Low Voltage	V_{IL}	0.3		0.8	VDC	
Input Low Current	I_{IL}	–	–	40	µA	
Input Leakage Current	I_{IN}	–	–	±2.5	µADC	V_{IN} = 0 to +5V, V_{CC} = 5.25V
Output High Voltage	V_{OH}		–	–	VDC	
Type OA		3.5	–	V_{CC}		I_{LOAD} = – 100 µA
Type OD						I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				VDC	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OD		–	–	0.75		I_{LOAD} = 15 mA
Three-State (Off) Current	I_{TSI}			±10	µADC	V_{IN} = 0.4 to V_{CC}-1

Table 2-4. Analog Electrical Characteristics

Signal Name	Type	Characteristic	Value
RIN	I (DA)	Input Impedance	> 70K Ω
		AC Input Voltage Range	1.1 VP-P
		Reference Voltage	+2.5 VDC
TXA1, TXA2	O (DD)	Minimum Load	300 Ω
		Maximum Capacitive Load	0 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	2.2 VP-P (with reference to ground and a 600 Ω load)
		Reference Voltage	+2.5 VDC
		DC Offset Voltage	± 200 mV
SPKR	O (DF)	Minimum Load	300 Ω
		Maximum Capacitive Load	0.01 µF
		Output Impedance	10 Ω
		AC Output Voltage Range	2.2 VP-P
		Reference Voltage	+2.5 VDC
		DC Offset Voltage	± 20 mV

Table 2-5. Current and Power Requirements

Mode	Current (ID)		Power (PD)		Notes
	Typical Current (mA) @ 25°C	Maximum Current (mA) @ 0°C	Typical Power (mW) @ 25°C	Maximum Power (mW) @ 0°C	
Normal mode	134	160	700	840	
Sleep mode	13	17	65	90	

Notes:

Test conditions:

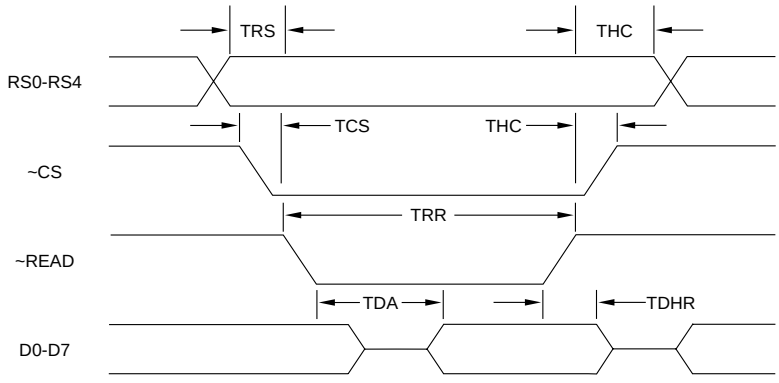
1. VCC = 5.0 VDC for typical values; VCC = 5.25 VDC for maximum values.
2. Input Ripple ≤ 0.1 Vpeak-peak.

Table 2-6. Absolute Maximum Ratings

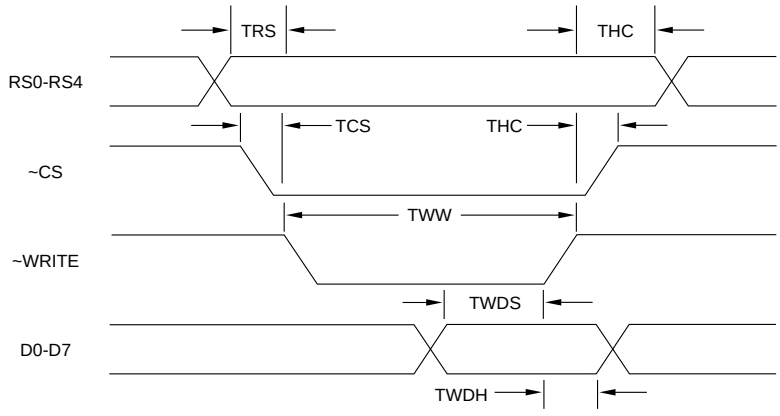
Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to (+5VD +0.5)	V
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (+5VA + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (+5VD + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA

Table 2-7. Host Bus Interface Timing

Parameter	Symbol	Min.	Max.	Units
a. Read				
Address Setup	TRS	10	–	ns
Chip Select Setup	TCS	0	–	ns
Control Hold	THC	10	–	ns
Read Data Access	TDA	-	35	ns
Read Data Hold	TDHR	10	–	ns
Read Pulse Width	TRR	45	–	ns
b. Write				
Address Setup	TRS	10	–	ns
Chip Select Setup	TCS	0	–	ns
Control Hold	THC	10	–	ns
Write Data Setup	TWDS	10	–	ns
Write Data Hold	TWDH	10	–	ns
Write Pulse Width	TWW	45	–	ns



a. Host Bus Read



b. Host Bus Write

* A minimum delay of 3 times the YCLK cycle time is required from the rising edge of ~WRITE to the falling edge of the next selected ~READ or ~WRITE. YCLK = crytstal frequency/2.

A minimum delay of 20 ns is required from the rising edge of ~READ to the falling edge of the next selected ~READ or ~WRITE.

1026F2-7 PIF WF

Figure 2-3. Host Bus Interface Waveforms

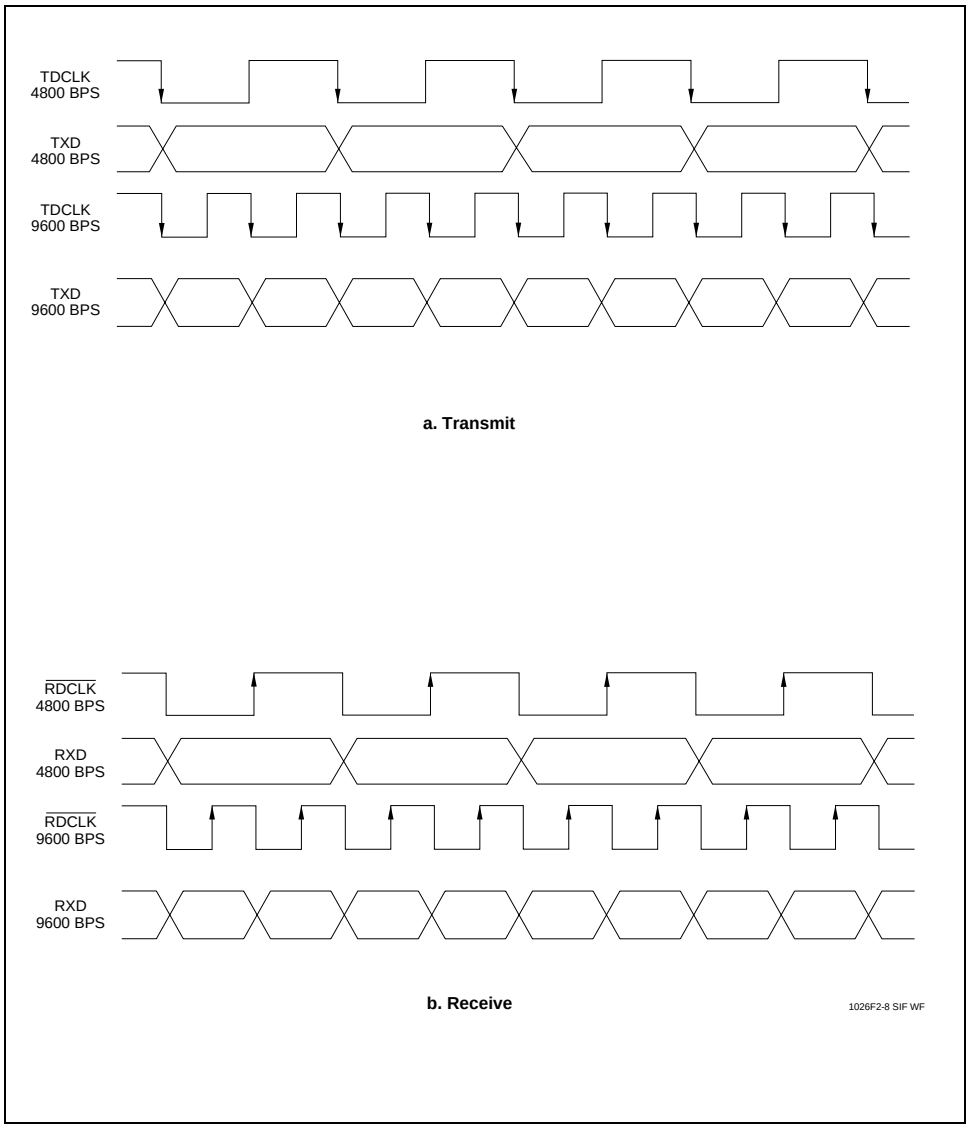


Figure 2-4. DTE Serial Interface Waveforms

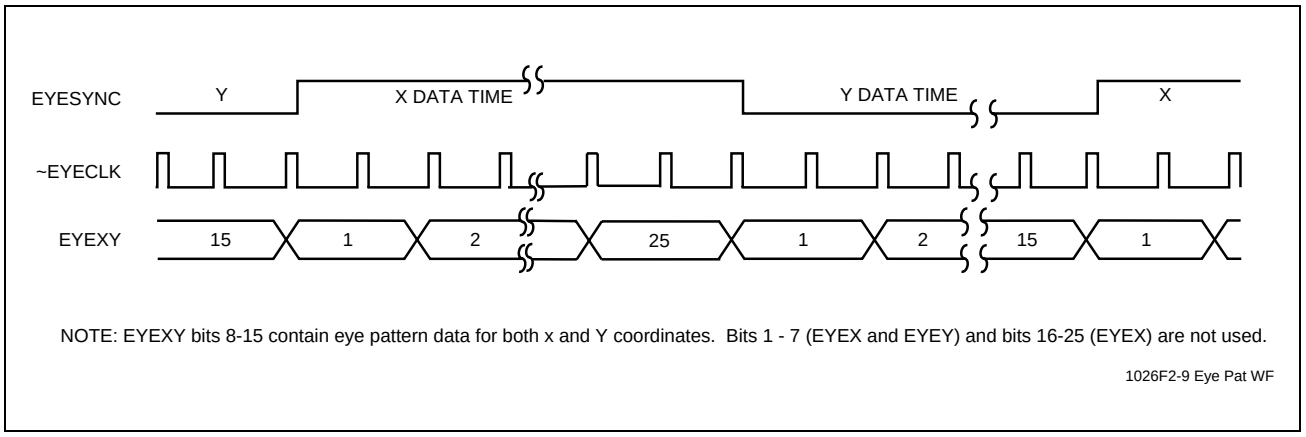


Figure 2-5. Eye Pattern Timing

2.2 LINE TRANSFORMER REQUIREMENTS FOR V.34

V.34 places high requirements upon the Data Access Arrangement (DAA) to the telephone line. The designer must, therefore, ensure that the total harmonic distortion seen at the RXA input to the modem be at least 45 dB below the minimum level of received signal. Due to the wider bandwidth requirement at a symbol rate of 3429 baud, the DAA must maintain linearity from 150 Hz to 3950 Hz.

Note that the major source of non-linear distortion in a DAA is the line transformer. A suitable line transformer is the MIDCOM 671 or equivalent.

3. SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in the modem DSP.

3.1 INTERFACE MEMORY

The modem DSP communicates with the host processor by means of a dual-port interface memory. The interface memory contains thirty-two 8-bit registers, labeled register 00 through 1F. Each register can be read from, or written into, by both the host and the DSP. The host communicates with the modem (DSP) interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

3.1.1 Interface Memory Map

An interface memory map of the 32 addressable registers in the modem is shown in Figure 3-1. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory.

	Bit							
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
1D	MEACC	MEACC1	MEMW	MEMCR	Memory Access Address High B-8 (MEADDH)			
1C	Memory Access Address Low B7-B0 (MEADDL)							
1B	EDET	DTDET	OTS	DTMFD	DTMFW			
1A	SFRES	RIEN	RION	DMAE	—	—	—	—
19	Memory Access Data MSB BF-B8 (MEDAM)							
18	Memory Access Data LSB B7-B0 (MEDAL)							
17	V.34 Transmit Status (SECTXB)							
16	V.34 Receive Status (SECRXB)							
15	SLEEP	—	RDWK	HWRWK	—	—	EXL3	EARC
14	ABCODE							
13	TLVL				RTH		TXCLK	
12	Configuration (CONF)							
11	BRKS	—	—	—	—	V23HDX	TEOF	—
10	Transmit Data Buffer (TBUFFER)							
0F	RLSD	FED	CTS	DSR	RI	—	—	—
0E	—	BRKD	—	SPEED				
0D	P2DET	PNDET	—	—	—	—	TXFNF	—
0C	PCOFF	—	—	—	SDET	SNDET	RXFNE	—
0B	TONEA	TONEB	TONEC	ATV25	—	—	—	EQMAT
0A	PNSUC	FLAGDT	PE	FE	OE	CRCS	FLAGS	SYNCD
09	NV25	CC	DTMF	ORG	—	DATA	—	DTR
08	—	TPDM	V21S	—	—	—	RTRN	RTS
07	—	—	—	—	L3ACT	—	RA	MHLD
06	RTDIS	—	CCRTN	HDLC	—	—	—	—
05	—	—	—	TXSQ	CEQ	TTDIS	STOFF	—
04	RB	EQT2	—	FIFOEN	—	NRZIEN	TOD	STRN
03	EPT	SEPT	—	RLSDE	—	—	—	—
02	TDE	SQDIS	—	—	—	—	—	—
01	VOLUME		—	—	—	TXHF	RXHF	—
00	Receive Data Buffer (RBUFFER)							

Notes:

1. — in the "Bit" columns indicates reserved for modem use only.

Figure 3-1. Modem Interface Memory Map

3.1.2 Interface Memory Signal Definitions

The individual bits in the interface memory are defined in Table 3-1. The bits in the interface memory are referred to using the format Z:Q. The register number is specified by Z (00 through 1F) and the bit number by Q (0 through 7, 0 = LSB).

Table 3-1. Interface Memory Bit Definitions

Mnemonic	Location	Default	Name/Description
ABCODE	14:0–7	00	**Abort Code.** If the handshake fails, an abort code is written into ABCODE. This code indicates the point in the handshake where the failure occurred. The abort code is not cleared by the modem but may be cleared by the host after it has been read. The abort codes and their meanings are listed in Table 3-2. Refer to ITU-T recommendations for meanings of the signal mnemonics used. (V.8, V.34)
ATV25	0B:4	–	**V25 Answer Tone Detector.** When set, status bit ATV25 signifies that the modem receiver detected a 2100 Hz answer tone. The bit is set when the answer tone is detected, and is reset when the tone ends. ATV25 is only active when the DATA bit is reset before energy is present at RXA and the modem is in originate mode. [V.8, V.23, and V.21; and tone modes (CONF = 80h, 81h, or 83h)]
BRKD	0E:6	–	**Break Detected.** When set, status bit BRKD indicates the modem is receiving continuous space in a synchronous mode. When reset, continuous space is not being received.
BRKS	11:7	0	**Break Sequence.** When control bit BRKS is set the modem will send continuous space. When BRKS is reset, the modem will transmit parallel data from the TBUFFER. (This bit is valid only when TPDM = 1.)
CC	09:6	0	**Control Channel.** In V.34 half-duplex modes, control bit CC is used to indicate the desired receive control channel date rate. CC =1 2400 bps CC = 0 1200 bps The actual rate used depends on the asymmetric bit settings in both modems. Bit 6 in $3DF must be set to 1 in both modems to allow control channel asymmetric data rates.
CCRTN	06:5	0	**Control Channel Retrain.** n V.34 half-duplex modes, either the source or the recipient modem may initiate a control channel retrain by setting bit CCRTN. Bit CCRTN should only be set when the modem is in control channel mode. The modem will reset bit CCRTN when the retrain process is complete. The retrain process can be monitored by observing SECRXB and SECTXB.
CEQ	05:3	1	**Compromise Equalizer Enable.** When control bit CEQ is set, the transmitter's digital compromise equalizer (or pre-emphasis for V.34 modes) is inserted into the transmit path. CEQ should be reset during analog loopback, tone, V.21 Channel 2, V.21, and V.23/75TX modes to ensure uniform transmit levels for both mark and space frequencies. CEQ must be set for V.8 and V.34 modes. In all modes, the modem programs the compromise equalizer taps. In V.17, V.29, and V.27 fax modes, the host may reprogram the compromise equalizer taps through RAM function 1 (Section 4).

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
CONF	12:0–7	AA	**Modem Configuration.** The CONF control bits select the modem configuration from the following codes:

Mode	Data Rate	CONF (Hex)	Setup (ms)
V.8		AA	
V.34 TCM	33600	CE	< 10
V.34 TCM	31200	CD	< 10
V.34 TCM	28800	CC	< 10
V.34 TCM	26400	CB	< 10
V.34 TCM	24000	CA	< 10
V.34 TCM	21600	C9	< 10
V.34 TCM	19200	C8	< 10
V.34 TCM	16800	C7	< 10
V.34 TCM	14400	C6	< 10
V.34 TCM	12000	C5	< 10
V.34 TCM	9600	C4	< 10
V.34 TCM	7200	C3	< 10
V.34 TCM	4800	C2	< 10
V.34 TCM	2400	C1	< 10
V.34 Cleardown	—	C0	
V.33 TCM	14400	31	< 15
V.33 TCM	12000	32	< 15
V.33 TCM	9600	34	< 15
V.33 TCM	7200	38	< 15
V.17 TCM	14400	B1	< 20
V.17 TCM	12000	B2	< 20
V.17 TCM	9600	B4	< 20
V.17 TCM	7200	B8	< 20
V.29	9600	14	< 20
V.29	7200	12	< 20
V.29	4800	11	< 20
V.27 ter	4800	02	< 50
V.27 ter	2400	01	< 50
V.23	1200TX/75 RX	A4	
V.23	75TX/1200 RX	A1	
V.21	0-300	A0	
V.21 Channel 2	300	A8	< 40
Transmit Single Tone	—	80	See Note 1
Transmit Dual Tone	—	83	See Note 1
Dialing	—	81	
DTMF Receiver	—	86	

NOTES:

1. The modem transmits one or two tones depending upon the selected mode. The tone frequencies and levels are host programmable in DSP RAM.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
CRCS	0A:2	0	**CRC Sending**. When set, status bit CRCS indicates that the transmitter is sending the CRC (2 bytes) in HDLC (SDLC) mode. A 0 indicates that the CRC is not being sent. Either a 16-bit (default) or 32-bit CRC may be sent as selected by the ITU-T CRC32 parameter in RAM (see Section 4.4, Function 52).
CTS	0F:5	–	**Clear To Send.** Status bit CTS is used to indicate that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted. CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 1-2. The CTS OFF-to-ON response time is programmable in DSP RAM.
DATA	09:2	1	**Data.** Control bit DATA is used to prevent the transmitter from entering and proceeding with the handshake (start-up) sequence and to ignore all V.24 interface signals. When control bit DATA is reset, the modem is prevented from entering and proceeding with the handshake (start-up) sequence and will ignore all V.24 interface signals. This bit should be set by the host at a suitable time after completion of dialing or answering.
DMAE	1A:4	0	**DMA Signals Enabled.** When set to a 1, control bit DMAE converts the ~RI and ~DSR output lines to the TXRQ (Transmitter Request) and RXRQ (Receiver Request) output lines, respectively. TXRQ is a high active signal that follows the state of the TDBE bit and the RXRQ is a high active signal that follows the state of the RDBF bit.
DSR	0F:4	–	**Data Set Ready.** When set (ON), status bit DSR indicates that the modem is in the data transfer state. When reset (OFF), DSR indicates that the DTE is to disregard all signals appearing on the interchange circuits except ~RI. DSR will switch to the OFF state when the modem is in a test mode.
DTDET	1B:6	–	**Dual Tone Detected.** When configured as a DTMF Receiver, the modem sets status bit DTDET when a signal is received that satisfies all DTMF criteria except on-time, off-time, and cycle-time. The encoded DTMFW Output Word (1B:0-3) value is available when DTDET is set.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

<table>
<tr><th>Mnemonic</th><th>Location</th><th>Default</th><th>Name/Description</th></tr>
<tr><td>DTMF</td><td>09:5</td><td>1</td><td>DTMF Select. When the modem is configured for dialing mode (CONF = 81h), the modem will dial using DTMF tones or pulses. When control bit DTMF is set, the modem will dial using DTMF tones. When DTMF is reset, the modem will dial using pulses. The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. When in dialing mode, the data placed in the Transmit Data Buffer is treated as digits to be dialed. The number to be dialed must be represented by two hexadecimal digits (e.g., if a 9 is to be dialed, then a 09 must be written to the Transmit Data Buffer). Also, see TDBE bit.

Dialing timing and power levels are host programmable in DSP RAM (Table 4-1).

Pulse dialing defaults to the ~OHRC output. The pulse dialing output is controlled by bit 6 in RAM address 0D4 (0 = ~OHRC output; 1 = ~TALK output) when in dial mode. The output may be selected using RAM access method 1 (see Section 4).</td></tr>
<tr><td>DTMFD</td><td>1B:4</td><td>–</td><td>DTMF Signal Detected. When configured as a DTMF receiver, the modem sets status bit DTMFD when a DTMF signal has been detected that satisfies all specified DTMF detect criteria.</td></tr>
<tr><td>DTMFW</td><td>1B:0-3</td><td>–</td><td>DTMF Output Word. When the modem is configured as a DTMF receiver and status bit DTDET is set by the modem, the encoded DTMF output is written into DTMFW.

<table>
<tr><th>DTMF Symbol</th><th>Encoded Output (Hex)</th><th>DTMF Symbol</th><th>Encoded Output (Hex)</th></tr>
<tr><td>0</td><td>0</td><td>8</td><td>8</td></tr>
<tr><td>1</td><td>1</td><td>9</td><td>9</td></tr>
<tr><td>2</td><td>2</td><td>*</td><td>A</td></tr>
<tr><td>3</td><td>3</td><td>#</td><td>B</td></tr>
<tr><td>4</td><td>4</td><td>A</td><td>C</td></tr>
<tr><td>5</td><td>5</td><td>B</td><td>D</td></tr>
<tr><td>6</td><td>6</td><td>C</td><td>E</td></tr>
<tr><td>7</td><td>7</td><td>D</td><td>F</td></tr>
</table></td></tr>
<tr><td>DTR</td><td>09:0</td><td>0</td><td>Data Terminal Ready. In V.8 and V.34 modes, control bit DTR is used to initiate a handshake sequence in originate mode when the DATA bit is set, or to immediately send answer tone in answer mode.

In V.21 and V.23 modes, control bit DTR must be set for the modem to enter data state when DATA bit is set. If in answer mode, the transmitter will send answer tone.

During the data mode, resetting DTR will cause the transmitter to turn off. The DTR bit parallels the operation of the hardware ~DTR control input. These inputs are ORed by the modem.</td></tr>
<tr><td>EARC</td><td>15:0</td><td>0</td><td>Extended Automatic Rate Change. Control bit EARC is used to enable automatic rate adaptation. (See Section 4 for detailed information about auto rate adaptation.) (V.34).</td></tr>
<tr><td>EDET</td><td>1B:7</td><td>–</td><td>DTMF Early Detection. When configured as a DTMF receiver, the modem sets status bit EDET to indicate that the received signal is probably a DTMF signal.</td></tr>
</table>

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
EPT	03:7	0	**Echo Protector Tone Enable.** When control bit EPT is set, an unmodulated carrier is transmitted for 185 ms (SEPT = 0) or 30 ms (SEPT = 1) followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is reset, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence. (V.33, V.17, V.29, V.27) The echo protector tone is typically used in V.27 ter and V.29 over dial-up lines. The tone is sent prior to the training sequence to ensure that the echo suppressers are pointing in the correct direction.
EQMAT	0B:0	0	**EQM Above Threshold.** Status bit EQMAT indicates that the measured EQM is above (1) or not above (0) the threshold value programmed in DSP RAM. The default threshold is 3000h. This bit is not cleared automatically by the modem after being set. The host must clear this bit to continue to monitor. (See Section 4.6.)
EQT2	04:6	1	**Equalizer T/2 Spacing Select.** When set, control bit EQT2 selects the receiver's adaptive equalizer spacing to be T/2 fractionally spaced, When reset, T spacing (T = 1 baud time) is selected. The use of T/2 is recommended over lines with severe amplitude distortion. (V.34)
EXL3	15:1	0	**External Loop 3 Selector.** When control bits L3ACT and EXL3 are both set, the signal path for local analog loopback is external to the modem (by connecting TXA and RXA together). When L3ACT is set but EXL3 is reset, the local analog loop signal path is internal to the modem. (This bit is useful for measuring the transmit spectrum in V.34 mode without having to connect to a remote modem.)
FE	0A:4	0	**Framing Error.** When set, status bit FE indicates that an ABORT sequence was detected in SDLC/HDLC synchronous mode. When reset, no framing error is detected.
FED	0F:6	–	**Fast Energy Detector.** When status bit FED is set, energy in the passband above the selected receiver threshold has been detected (see RTH). DTR must be on in order for FED to function in full duplex modes (DATA = 1).
FIFOEN	04:4	0	**FIFO Enable.** When control bit FIFOEN = 1 and TPDM = 1, the host can input up to 16 bytes of data through TBUFFER, using the TDBE bit as a software interrupt or the TXRQ signal (DMAE = 1) as a DMA request interrupt. The Receive FIFO is always enabled. The host may wait up to 16 byte-times before reading the data in RBUFFER. The RDBF bit or RXRQ signal (DMAE = 1) signals the availability of receive data to the host. The trigger level for RDBF bit/RXRQ signal is host programmable in DSP RAM. (See Section 4 for a detailed description about FIFO operation.)
FLAGDT	0A:6	–	**V.21 Channel 2 Flag Detected.** When set, status bit FLAGDT indicates that V.21 Channel 2 Flags (7Eh) are being detected. (V.33, V.17, V.29, V.27 ter)
FLAGS	0A:1	0	**Flag Sequence.** When set, status bit FLAGS indicates that the transmitter is sending the Flag sequence in SDLC/HDLC mode. When reset, FLAGS indicates that the transmitter is sending data.
HDLC	06:4	0	**HDLC Select.** When control bit HDLC is set, HDLC operation is enabled. When HDLC is reset, HDLC operation is disabled. The TDBE bit must be 1 prior to setting HDLC to a 1. The HDLC bit is valid only in parallel data mode (TPDM = 1). Not valid in FSK modes except V.21 channel 2. RTS must be off before switching in or out of HDLC mode while in DATA mode.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
HWRWK	15:4	1	**Host Write Wake up.** When control bit HWRWK is set and the modem is in sleep mode, a host write to any register with the exception of 1D:0-7, will bring the modem out of sleep mode. (See SLEEP bit.)
L3ACT	07:3	0	**Loop 3 Activate.** When control bit L3ACT is set, the transmitter's analog output is coupled internally to the receiver's analog input through an attenuator (local analog loopback) in accordance with ITU-T Recommendation V.54. Optionally, the signal path for loop 3 can also be established externally to the modem (see EXL3). The modem may only be placed into loop 3 mode when in idle mode (~DTR signal is OFF and the DTR bit is reset). NEWC must be set after any change in the L3ACT bit. The loopback is then completed (terminated) by asserting ~DTR signal ON (low) or setting the DTR bit.
MEACC	1D:7	0	**Memory Access Enable.** When control bit MEACC is set, the DSP accesses the RAM associated with the address in MEADDH and MEADDL. The MEMW bit determines if a read or write is performed. The DSP resets the MEACC upon RAM access completion.
MEACC1	1D:6	0	**Memory Access Enable.** The MEACC1 bit is used to access DSP RAM locations $C00-$C5F. (See paragraph 4.2.)
MEADDL	1C:0–7	00	**Memory Access Address Low (7-0).** MEADDL contains the lower 8 bits (bits 7-0) of the address used to access modem RAM via the memory access data LSB (18) and MSB (19) registers. (See Table 4-1.)
MEADDH	1D:0–3	0	**Memory Access Address High (B-0).** MEADDH contains the upper 8 bits (bits B-8) of the address used to access modem RAM via the memory access data LSB (18) and MSB (19) registers. (See Table 4-1.)
MEDAL	18:0–7	00	**Memory Data LSB.** MEDAL is the least significant byte (bits 7-0) of the 16-bit data word used in reading or writing data locations in modem RAM.
MEDAM	19:0–7	00	**Memory Data MSB.** MEDAM is the most significant byte (bits F-8) of the 16-bit data word used in reading or writing data locations in modem RAM.
MEMCR	1D:4	0	**Memory Continuous Read.** When set to a 1, control bit MEMCR instructs the DSP to automatically update the data in MEDAM and MEDAL based on the RAM address in MEADDH and MEADDL. without the host having to set the MEACC bit. The modem will set the NEWS bit to a 1 when new data is available.
MEMW	1D:5	0	**Memory Write.** When MEMW is set and MEACC is set, the DSP copies data from the interface memory data registers MEDAL (18) and MEDAM (19) into the memory location addressed by MEADDL and MEADDH. When control bit MEMW is reset and MEACC is set, the DSP reads memory at the location addressed by MEADDL and MEADDH. The read data is stored into interface memory data registers MEDAL (18) and MEDAM (19).
MHLD	07:0	0	**Mark Hold.** When control bit MHLD is set, the transmitter's digital input data is clamped to a mark. When MHLD is reset, the transmitter's input is taken from TXD or TBUFFER (see TPDM).

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
NCIA	1F:6	–	**NEWC Interrupt Active.** When the new configuration chip 0 interrupt is enabled (NCIE is set) and a new configuration is implemented (NEWC is reset), the modem asserts IRQ and sets status bit NCIA to indicate that NEWC being reset caused the interrupt. NCIA and the interrupt request due to NEWC are cleared by the host writing a 0 into NCIE. (See NEWC and NCIE.)
NCIE	1F:2	0	**NEWC Interrupt Enable.** When control bit NCIE is set (interrupt enabled), the modem will assert IRQ and set NCIA when the NEWC bit is reset by the modem. When NCIE is reset (interrupt disabled), NEWC has no effect on IRQ or NCIA. (See NEWC and NCIA.)
NEWC	1F:0	0	**New Configuration.** Control bit NEWC must be set by the host after the host changes the configuration code in CONF (register 12) or changes any of the following controls bits: CEQ (05:3), DTMF (09:5), EQT2 (04:6), L3ACT (07:3), ORG(09:4), RTH (13:2,3), SFRES (1A:7), SLEEP (15:7), TLVL (13:4-7), TXCLK (13:0-1), or V21S (08:5).This informs the modem to implement the new configuration. The modem resets the NEWC bit when the configuration change is implemented. A configuration change can also cause IRQ to be asserted. (See NCIE and NCIA.)
NEWS	1F:3	–	**New Status.** When set, status bit NEWS indicates that one or more status bits located in registers 0A–0F, 01, 12, 14, 16-17, 1A, or 1B have changed state (default = interrupt OFF), or a DSP RAM read or write has been completed (default = interrupt ON). This bit can be reset only by the host. The host may mask the effect of individual status bits upon NEWS by writing a mask value to DSP RAM (see Function 17 in Section 4). When set, this bit can cause IRQ to be asserted. (See NSIE and NSIA.) **NOTE:** When read/modifying register 1F, set NEWS = 1 to ensure that the host does not reset NEWS after the modem DSP has set NEWS during read/modify. If NEWS = 0, setting NEWS to a 1 will not be accepted by the DSP and NEWS will remain a 0.
NRZIEN	04:2	0	**NRZI Enable.** When set, control bit NRZIEN enables NRZI transmitter encoding and receiver decoding in all synchronous HDLC modes. When NRZIEN is reset, NRZ encoding and decoding is used.
NSIA	1F:7	–	**NEWS Interrupt Active.** When the new status interrupt is enabled (NSIE is set) and a change of status occurs (NEWS is set), the modem asserts IRQ and sets status bit NSIA to indicate that NEWS being set caused the interrupt. NSIA and the interrupt request due to NEWS are cleared when the host writes a 0 to NEWS. (See NEWS and NSIE.)
NSIE	1F:4	0	**NEWS Interrupt Enable.** When control bit NSIE is set (interrupt enabled), the modem will assert IRQ and set NSIA when NEWS is set by the modem. When NSIE is reset (interrupt disabled), NEWS has no effect on IRQ or NSIA. (See NEWS and NSIA.)
NV25	09:7	0	**No V.25 Answer Tone.** When control bit NV25 is set, the modem will not transmit the 2100 Hz ITU-T answer tone when a handshake sequence is initiated and the modem is in answer mode.
OE	0A:3	0	**Overrun Error.** When set, status bit OE indicates a receiver overrun condition occurred. That byte causing the overrun and all others that follow will not be placed into the RXFIFO as long as the RXFIFO is full. This bit must be reset by the host.
ORG	09:4	0	**Originate.** When configuration bit ORG is set, the modem is in originate mode; when reset, the modem is in answer mode. Since this is a configuration bit, the NEWC bit must be set after any change in the ORG bit.
OTS	1B:5	–	**DTMF On-Time Satisfied.** When configured as a DTMF receiver, the modem sets status bit OTS after the on-time criteria is satisfied. This bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy the DTMF off-time criteria.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
P2DET	0D:7	0	**P2 Sequence Detected.** When status bit P2DET is set, the modem is detecting the P2 portion of the training sequence. When P2DET is reset, P2 is not being detected. (V.33, V.17, V.29. V.27)
PCOFF	OC:7	0	This bit is set when at least 40 binary ones were found during the 35 ms sequence that precedes a Primary Channel turn off, and serves as a Primary Channel turn off indicator. It is also set when 40 binary ones were found during CC turn off. The flag remains on after the PC to CC transition and has to be reset by the host if necessary. However for the CC to PC transition, the bit is automatically cleared as the modem enters PC.
PE	0A:5	0	**CRC Error.** When set, status bit PE indicates a bad CRC was detected in the SDLC/HDLC synchronous mode. When reset, a frame with a good CRC was received.
PNDET	0D:6	–	**PN Sequence Detected.** Status bit PNDET indicates that the PN portion of the training sequence is being detected (set) or is not being detected (reset). (V.33, V.17, V.29. V.27 ter)
PNSUC	0A:7	0	**PN Success.** When status bit PNSUC is set, the modem has successfully trained at the end of the PN portion of the high speed training sequence. When PNSUC is reset, a successful training has not occurred. (V.33, V.17, V.29. V.27 ter) In V.34 half-duplex mode, PNSUC is set by the modem when at least 40 ones have been received by the source modem. The host must reset this bit. This bit is not buffered in the receive FIFO, so the host must read any remaining data in RBUFFER.
RA	07:1	0	**Relay A Activate.** When control bit RA is set, the ~OHRC output (~RLYA) is active; when reset, the ~OHRC output is off (high).
RB	04:7	0	**Relay B Activate.** When control bit RB is set, the ~TALK output (~RLYB) is active; when reset, the ~TALK output is off (high).
RBUFFER	00:0–7	–	**Receive Data Buffer.** The host obtains channel data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER. The RBUFFER contains the received data when the RDBF bit is set. (See RDBF, RDBIE, and RDBIA.)
RDBF	1E:0	–	**Receive Data Buffer Full.** When set, status bit RDBF signifies that the receiver wrote valid data into RBUFFER (register 00). This condition can also cause IRQ to be asserted. The host reading RBUFFER resets the RDBF and RDBIA bits. (See RDBIE and RDBIA.)
RDBIA	1E:6	–	**Receive Data Buffer Interrupt Active.** When the receive data buffer interrupt is enabled (RDBIE is set) and RBUFFER (register 00) is written to by the modem (RDBF is set), the modem asserts IRQ and sets RDBIA to indicate that RDBF being set caused the interrupt. The host reading RBUFFER resets the RDBIA bit and clears the interrupt request due to RDBF. (See RDBF and RDBIE.)
RDBIE	1E:2	0	**Receive Data Buffer Interrupt Enable.** When control bit RDBIE is set (interrupt enabled), the modem will assert IRQ and set the RDBIA bit when RDBF is set by the modem. When RDBIE is reset (interrupt disabled), RDBF has no effect on IRQ or RDBIA. (See RDBF and RDBIA.)
RDWK	15:5	1	**Ring Detect Wake up.** When control bit RDWK is set and the modem is in sleep mode, an incoming ring signal on the RINGD pin will bring the modem out of sleep mode. The RINGD pin must be normally low for the RDWK function to work. (See SLEEP bit).

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RI	0F:3	–	**Ring Indicator.** When set, status bit RI indicates that a ringing signal is being detected. Ringing is detected if pulses are present on the RINGD input in the 15 Hz–68 Hz frequency range. The RI bit follows the ringing signal with a 1 during the ON time and a 0 during the OFF time coincident with ~RI output signal. The decision bounds are host programmable in DSP RAM. This bit is valid only when DATA bit is reset and is not applicable in tone modes.
RIEN	1A:6	0	**RION Enable.** When control bit is a 1, the ~RI output will reflect the RION bit. When a 0, the ~RI output follows the ringing signal on the RINGD input.
RION	1A:5	0	**Ring Indicator On.** Control bit RION determines the state of the ~RI output (1 = low; 0 = high) when bit RIEN is set and the DATA bit is reset.
RLSD	0F:7	–	**Received Line Signal Detector.** When status bit RLSD is set, the modem has finished receiving the training sequence or has turned on due to detected energy above threshold, and is receiving data. RLSD is reset when the modem is in the idle state and during the reception of a training sequence. The RLSD threshold may be adjusted in DSP RAM.
RLSDE	03:4	1	**RLSD Enable.** When control bit RLSDE is set, the ~RLSD pin reflects the RLSD bit state. When RLSDE is reset, the ~RLSD pin is clamped OFF and data is clamped to a mark regardless of the state of the RLSD bit.
RTDIS	06:7	0	**Receiver Training Disable.** When control bit RTDIS is set, the modem is prevented from recognizing a training sequence and entering the training state. When RTDIS is reset, receiver training is enabled. (V.17, V.29, V.27)
RTH	13:2,3	0	**Receiver Threshold.** The RTH control bits select the receiver energy detector threshold according to the following codes: **RTH** **RLSD ON** **RLSD OFF** 0 – 43 dBm – 48 dBm 1 – 33 dBm – 38 dBm 2 – 26 dBm – 31 dBm 3 – 16 dBm – 21 dBm
RTRN	08:1	0	**PC Retrain.** In v.34 half-duplex mode of the recipient modem this bit is used to initiate a primary channel (PC) retrain. Note that PC retrain is not recommended by ITU-T.30.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
RTS	08:0	0	**Request to Send.** Control bit RTS is used to enable the modem to transmit any data on TXD when CTS becomes active. The RTS bit parallels the operation of the ~RTS hardware control input. These inputs are ORed by the modem. (See CTS and DTR bits.) In V.23 and V.21 constant carrier modes, RTS controls data transmission and DTR controls the carrier. In V.23 and V.21 controlled carrier modes, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, CTS is turned ON per Table 1-2. In V.34 HD mode, setting bit RTS switches from control channel to primary channel mode. Resetting RTS switches to control channel mode.
RXFNE	0C:1	-	**Receiver FIFO Not Empty.** When set, status bit RXFNE indicates that the receiver FIFO contains one or more bytes of data. When reset, bit RXFNE indicates that the receiver FIFO is empty. (TPDM = 1, FIFOEN = 1)
RXHF	01:1	0	**Receiver FIFO Half Full.** When set, status bit RXHF indicates that there are 8 or more bytes in the 16-byte Receiver FIFO buffer. When reset, RXHF indicates that there are less than 8 bytes in the Receiver FIFO buffer. (TPDM = 1) An interrupt mask is available to allow an interrupt request to be generated when RXHF is set (see Function 17 in Section 4).
SDET	0C:3	0	**S Detector.** When set, status bit SDET indicates that an S sequence has been detected. This bit is reset by the modem at the end of the S sequence (V.34 mode).
SECRXB	16:0-7	–	**Secondary Receive Buffer.** The host obtains V.8/V.34 receive handshake status information from the modem receiver by reading a data byte from the SECRXB.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
SECTXB	17:0-7	–	**Secondary Transmit Buffer.** The host obtains V.34 transmit handshake status information.
SEPT	03:6	0	**Short Echo Protector Tone.** When control bit SEPT is set, the echo protector tone duration is 30 ms; when reset, the echo protector tone duration is 185 ms. (V.33, V.17, V.29, V.27)
SFRES	1A:7	0	**Soft Reset.** When control bit SFRES is set to a 1, the modem will perform power-on reset processing. The NEWC bit will be reset to a 0 by the modem upon completion of the reset processing. NEWC must be set to initiate the reset. Wait for NEWC to clear before accessing the modem.
SLEEP	15:7	0	**Sleep Mode.** When control bit SLEEP is set, the modem is placed in sleep mode for reduced power consumption and the SLEEP pin is driven low. The modem can be awakened only if bit RDWK and/or HWRWK is set. If both RDWK and HWRWK are reset, only a power-on-reset will bring the modem out of sleep mode. The modem is reset upon wake up.
SNDET	0C;2	0	**S Negative Detector.** When set, status bit SNDET indicates that a ***S*** (here ***S*** indicates an S with a bar above, per ITU notation) sequence has been detected. This bit is reset at the end of the ***S*** sequence (V.34 mode).
SPEED	0E:0–4	–	**Speed Indication.** In non-V.34 modes, the SPEED status bits indicate the receiver's and transmitter's data rate at the completion of a handshake. In V.34 mode, the SPEED status bits indicate the source modem's data rate and the CONF indicate the recipient modem's data rate at the completion of a handshake. For speed above 28800 bps, see Function 1 in Section 4. **SPEED (Hex) — Data Rate (bps)** 00 — 0–300 01 — 600 02 — 1200 03 — 2400 04 — 4800 05 — 9600 06 — 12000 07 — 14400 08 — 7200 09 — 16800 0A — 19200 0B — 21600 0C — 24000 0D — 26400 0E — 28800 0F — 31200 10 — 33600
SQDIS	02:6	0	**Squarer Disable (Tone Detector C).** When control bit SQDIS is set, the squarer in front of tone detector C is disabled; when reset, the squarer is enabled. Disabling the squarer cascades the prefilter and filter C creating an 8th-order filter.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
STOFF	05:1	0	**Soft Turn Off.** When control bit STOFF is set, the transmitter sends a tone at the end of a transmission in V.23 and V.21 configurations. This tone is detected as a mark frequency at the receiver. The soft turn off tone frequencies and durations are as follows: **Configuration** / **Frequency (Hz)** / **Duration (ms)** V.23/1200 — 900 — 7 V.21 Originate — 880 — 30 V.21 Answer — 1550 — 30
STRN	04:0	0	**Short Train Select.** When a V.17 or V.27 configuration is selected in CONF, control bit STRN selects the training mode (1 = short train; 0 = long train). (V.17, V.27 ter) STRN may be set only after the completion of a successful long train. STRN may be set or reset during data mode (RLSD on) or anytime before the start of the following training sequence. On the transmitter, setting STRN will force the following training sequence to be short train on the receiver. Setting STRN will inhibit the equalizer taps from being reset during the following short train thus allowing for a fast adaptation. A short train may be received only when STRN is set. Once STRN is set, the DATA bit must remain set and the only allowable configuration between V.17 and V.27 that will not alter the taps is V.21 Channel 2. (V.17, V.27 ter)
SYNCD	0A:0	0	**Sync Pattern Detected.** When set, status bit SYNCD indicates that SDLC/HDLC flags (7E pattern) are being detected. When reset, the 7E pattern is not being detected. This bit is valid only in SDLC/HDLC mode (HDLC = 1).
TBUFFER	10:0–7	00	**Transmit Data Buffer.** The host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER. The data is transmitted bit 0 first (see TDBE). **NOTE:** Do not read TBUFFER during data mode.
TDE	02:7	1	**Tone Detectors Enable.** When control bit TDE is set, tone detectors A, B, and C are enabled; when reset, tone detectors are disabled.
TDBE	1E:3	–	**Transmit Data Buffer Empty.** When set, status bit TDBE signifies that the modem has read TBUFFER (register 10) and the host can write new data into TBUFFER. This condition can also cause IRQ to be asserted. The host writing to TBUFFER resets the TDBE and TDBIA bits. If the host does not write new data into TBUFFER, the modem sends mark. TDBE must be a 1 before setting up HDLC modes. CTS must be on **before** data is loaded into TBUFFER. If FIFOEN is set, TDBE, when set, indicates that the transmit FIFO is empty. (See TDBIE and TDBIA.)
TDBIA	1E:7	–	**Transmit Data Buffer Interrupt Active.** When the transmit data buffer interrupt is enabled (TDBIE is set) and register 10 is empty (TDBE is set), the modem asserts IRQ and sets status bit TDBIA to indicate that TDBE being set caused the interrupt. The host writing to register 10 resets the TDBIA bit and clears the interrupt request due to TDBE. (See TDBIE and TDBE.)
TDBIE	1E:5	0	**Transmit Data Buffer Interrupt Enable.** When control bit TDBIE is set (interrupt enabled), the modem will assert IRQ and set the TDBIA bit when TDBE is set by the modem. When TDBIE is reset (interrupt disabled), TDBE has no effect on IRQ or TDBIA. (See TDBE and TDBIA.)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TEOF	11:1	0	**HDLC Transmit End of Frame.** When operating in HDLC with FIFOEN = 1, the host must set control bit TEOF to inform the transmitter that the corresponding data is the last byte in a frame. TEOF must be set prior to loading the last byte in TBUFFER. The host must reset TEOF prior to loading the next data byte.
TLVL	13:4–7	9	**Transmit Level.** The TLVL code selects the transmitter analog output level at the TXA pin as follows: **TLVL Code (Hex) — TX Output Level (dBm ±0.5 dB)** 0 — –0.0 1 — –1.0 2 — –2.0 3 — –3.0 4 — –4.0 5 — –5.0 6 — –6.0 7 — –7.0 8 — –8.0 9 — –9.0 A — –10.0 B — –11.0 C — –12.0 D — –13.0 E — –14.0 F — –15.0 The host can fine tune the transmit level by changing a value in DSP RAM. Changing TLVL requires that the NEWC bit be set.
TOD	04:1	0	**Train On Data.** When set, control bit TOD enables the train-on-data algorithm to converge the equalizer without a received training sequence. (V.27)
TONEA	0B:7	–	**Tone A Detected.** When set, status bit TONEA indicates that energy is present on the line within the tone detector A passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEB	0B:6	–	**Tone B Detected.** When set, status bit TONEB indicates that energy is present on the line within the tone detector B passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM.
TONEC	0B:5	–	**Tone C Detected.** When set, status bit TONEC indicates that energy is present on the line within the tone detector C passband and above its threshold. The bandpass filter coefficients are host programmable in DSP RAM. The TONEC filter is preceded by a squarer in order to facilitate detection of difference tones. This squarer may be disabled with the SQDIS bit (see SQDIS bit).
TPDM	08:6	0	**Transmitter Parallel Data Mode.** When control bit TPDM is set, the modem accepts data for transmission from the TBUFFER (register 10) rather than the TXD input. (See TDBE and RTS.) **Note:** The TPDM bit must be set to a 1 in HDLC mode (HDLC bit = 1).
TTDIS	05:2	0	**Transmitter Training Disable.** When control bit TTDIS is set, the transmitter does not generate the training sequence at the start of transmission. With training disabled, the RTS/CTS delay is less than two baud times. (V.33, V.17, V.29, V.27 ter)

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
TXCLK	13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock. NEWC must be set to initiate TXCLK change. The TXCLK encoding is: **TXCLK** **Transmit Clock** 0 Internal 2 External (XTCLK) 3 Slave (~RDCLK) When the external clock is selected, an external clock **must** be supplied to the XTCLK input pin. The external clock signal must have a duty cycle of 50% and must be within ±0.01% of the nominal TDCLK frequency (the actual frequency of TDCLK as measured when internal clock is selected). TDCLK will be phase locked to XTCLK when the external clock option is selected. When the slave clock is selected, the transmitter clock (TDCLK) is phase locked to the receiver clock (~RDCLK).
TXFNF	0D:1	-	**Transmitter FIFO Not Full.** When set, status bit TXFNF indicates that the transmitter FIFO is not full and the host may continue to write data to the TBUFFER. When reset, TXFNF indicates that the transmitter FIFO is full. (TPDM = 1, FIFOEN = 1)
TXHF	01:2	0	**Transmitter FIFO Half Full.** When set, status bit TXHF indicates that there are 8 or more bytes in the 16-byte Transmitter FIFO buffer. When reset, TXHF indicates that there are less than 8 bytes in the Transmitter FIFO buffer. (TPDM = 1, FIFOEN = 1) An interrupt mask is available to allow an interrupt request to be generated when TXHF is set (see Section 4, Function 17).
TXSQ	05:4	0	**Transmitter Squelch.** When control bit TXSQ is set, the transmitter analog output is squelched. All other transmitter functions continue as normal. When TXSQ is reset, the transmitter output functions normally. This bit is useful in 2-wire configurations where it is necessary to measure the spectrum and transmit level of a transmitter. Setting the TXSQ bit turns off the transmitter so that only one of the two carriers is present. After TXSQ is reset, a retrain should be sent to reestablish the data transfer. It is recommended that TXSQ be set while in the fax receive mode.
V21S	08:5	0	**V21 Synchronous.** In V.21 configuration (CONF = A0h), setting control bit V21S selects synchronous mode. In V.21 synchronous mode, a transmit clock is provided on the TDCLK pin and a receive clock is provided on the ~RDCLK pin. During transmit, synchronous data may be applied in either serial or parallel form depending on the TPDM bit. During receive, synchronous data is output in both serial or parallel form. NEWC must be set immediately after changing the V21S bit to initiate the mode change. **Note: Do not** set this bit in V.21 Channel 2 (CONF = A8h).
V23HDX	11:2	0	**V.23 Half Duplex.** Control bit V23HDX selects half-duplex or full-duplex operation in V.23.

Table 3-1. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Location	Default	Name/Description
VOLUME	01:6,7	0	**Volume Control.** The encoded VOLUME control bits select speaker off or one of three volume attenuation levels (at RIN) as follows: **7** **6** **Description** 0 0 Speaker off 1 0 Speaker attenuation = 0 dB (high volume) 0 1 Speaker attenuation = 6 dB (medium volume) 1 1 Speaker attenuation = 12 dB (low volume)

Table 3-2. ABCODE Error Code Definitions

Type	Mnemonic	Code	Description
RX	TimeOutWaitInfo0	$21	timeout waiting for INFO0
RX	CheckSumErrInfo0	$22	checksum error in INFO0
RX	TimeOutWaitTone	$23	timeout waiting for tone A or B
RX	TimeOutWaitPR1	$24	timeout waiting for first phase reversal
RX	TimeOutWaitProbEndTone	$25	timeout waiting for probing cut-off tone
RX	TimeOutWaitPR2	$26	timeout waiting for second phase reversal
RX	TimeOutWaitProbEnd	$27	timeout waiting for end of probing
RX	TimeOutWaitPR3	$28	timeout waiting for third phase reversal
RX	TimeOutWaitInfo1	$29	timeout waiting for INFO1
RX	CheckSumErrInfo1	$2A	checksum error in INFO1
RX	FoundToneBeforeINFO	$2B	found tone before INFO0
RX	FoundUnexpectedINFO	$2C	found unexpected INFO0
RX	TimeOutWaitRCCOFF	$31	timeout waiting for recipient control channel to turn off
RX	ErrorInFirstCCtrn	$91	error in first CC train
RX	TimeOutWaitPPh	$92	Time out waiting for PPh
RX	ToneDetCCRTN	$93	Tone A/B detected in CC retrain
RX	TimeOutWaitALT	$94	timeout waiting for ALT
RX	FoundACh	$95	found ACh
RX	FEDOffCC	$96	FED off during CC data
RX	TimeOutWaitCCOFF	$97	timeout waiting for CC turnoff
RX	Phase2GoRetrain	$A1	go out with unresolved problem in phase 2, force retrain
RX	ReScProblemWithS	$B0	problem with S-sequence in HDX-resync
RX	ReScFEDoffDuringS	$B1	FED off during S-sequence in HDX-resync
RX	ReScSgoneError	$B2	S-sequence gone before expected in HDX-resync
RX	ReScSSbarTimeOut1	$B3	timed out waiting for S-Sbar in HDX-resync
RX	ReScSSbarTimeOut2	$B4	timed out waiting for S-Sbar in HDX-resync
RX	ReScTimeOutWtForS	$B5	timed out waiting for S in HDX-resync
RX	ReScFailSyncUp	$B6	timed out syncing up with PP
RX	ECProblemWithS	$C0	problem with S-sequence in phase 3
RX	ECFEDoffDuringS	$C1	FED off during S-sequence in phase 3
RX	ECSgoneError	$C2	S-sequence gone before expected in phase 3
RX	ECSSbarTimeOut1	$C3	timed out waiting for S-Sbar in phase 3
RX	ECSSbarTimeOut2	$C4	timed out waiting for S-Sbar in phase 3
RX	ECTimeOutWtForS	$C5	timed out waiting for S in phase 3
RX	TrainTRNFail	$C7	Training on TRN failed
RX	ProblemWithS	$D0	problem with S-sequence in phase 4
RX	FEDoffDuringS	$D1	FED off during S-sequence in phase 4
RX	SgoneError	$D2	S-sequence gone before expected in phase 4
RX	SSbarTimeOut1	$D3	timed out waiting for S-Sbar in phase 4
RX	SSbarTimeOut2	$D4	timed out waiting for S-Sbar in phase 4
RX	TimeOutWtForS	$D5	timed out waiting for S in phase 4
RX	TimeOutWtForMP	$D6	timed out waiting for MP
RX	TimeOutWtForE	$D8	timed out waiting for E
RX	TimeoutTxRNEG	$DA	timed out in transmitter Rate reneg
RX	TimeoutTxMPh	$DB	timed out in transmitter MPh
RX	Ph2RetrainDet	$E2	retrain detected during phase 2
RX	Ph3RetrainDet	$E3	retrain detected during phase 3
RX	Ph4RetrainDet	$E4	retrain detected during phase 4
RX	DtrOff	$FE	DTR went off during training
RX	TxAbort	$FF	tx set abort flag
TX	InternalCommErr	$71	didn't get to write out first mapping frame

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4. DSP RAM ACCESS

The modem DSP contains a 16-bit wide random access memory (RAM). The host processor can access (read or write) the RAM through a 12-bit memory address in registers 1D and 1C.

4.1 INTERFACE MEMORY ACCESS TO DSP RAM

The interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The address stored in interface memory RAM address registers MEADDH and MEADDL by the host is the DSP RAM address for data access. The data is transferred through data registers MEDAM and MEDAL.

One or two bytes (1 byte = 8 bits) are transferred between DSP RAM and DSP interface memory once each device cycle. The DSP operates at a 7200 Hz sample rate.

The RAM access bit (MEACC) in the interface memory instructs the DSP to access the RAM. The transfer is initiated by the host setting the MEACC bit. The DSP tests this bit each sample period.

RAM can be accessed using one of four methods:

1. 8-bit read - 8-bit write.
2. 16-bit read - 8-bit write.
3. 16-bit read - 16-bit write.
4. 16-bit read only (modem diagnostics).

Parameters transferred under the first method have only 8 bits of significance. The data is written to and read from MEDAL. Data in MEDAM is ignored.

Parameters transferred using the second method have 16 bits of significance but can be written only 8 bits at a time. These parameters have two access codes associated with them, one for the least significant 8 bits and one for the most significant 8 bits. The host need read only the low address to obtain both the most significant and the least significant bytes of the data if the two access codes are in consecutive order.

Parameters transferred using the third method involve 16-bit read or write operations using one access code.

Finally, all diagnostic read operations using the fourth method use only one access code. Data is read from MEDAM and MEDAL.

The parameters available in DSP RAM are listed in Table 4-1.

4.2 HOST DSP READ AND WRITE PROCEDURES

DSP RAM Write Procedure

1. Set MEMW to inform the DSP that a RAM write will occur when MEACC is set.
2. Load the RAM address into the MEADDH and MEADDL registers.
3. Write the desired data into the interface memory RAM data registers MEDAM and/or MEDAL.
4. Set MEACC to signal the DSP to perform the RAM write.
5. When the DSP has transferred the contents of the interface memory RAM data registers into RAM, the modem resets the MEACC bit and sets the NEWS bit to indicate DSP RAM write completion. If the NSIE bit is a 1, IRQ is asserted and NSIA is set to inform the host that setting of the NEWS bit is the source of the interrupt request.
6. Upon the completion of IRQ servicing, write a 0 into the NEWS bit to clear the NSIA bit and to negate IRQ if no other interrupt requests are pending.

DSP RAM Read Procedure

1. Reset MEMW to inform the DSP that a RAM read will occur when MEACC is set.
2. Load the RAM address code into the MEADDH and MEADDL registers.
3. Set MEACC to signal the DSP to perform the RAM read.
4. When the DSP has transferred the contents of RAM into the interface memory RAM data registers MEDAM and/or MEDAL, the modem resets the MEACC bit and sets the NEWS bit to indicate DSP RAM read completion. If the NSIE bit is a 1, IRQ is asserted and NSIA is set to inform the host that setting of the NEWS bit is the source of the interrupt request.
5. Upon the completion of IRQ servicing, write a 0 into the NEWS bit to clear the NSIA bit and to negate IRQ if no other interrupt requests are pending.

Special DSP RAM Access

The DSP RAM addresses in the range of $C00 to $C3F have a unique access method. This address range is mapped to $800 - $83F when the MEMACC1 bit is set. When accessing this area the addresses $4800 - $483F must be used. When loading the RAM address code into the MEADDH register the mask $48 instead of $0C must be used in read-modify-write operations.

Shows a flowchart of a procedure to read EQM using method 4. Shows a flowchart of a procedure to enable DTMF in FSK modes.

4.3 RAM READ AND WRITE EXAMPLES

Figure 4-1 shows a flowchart of a procedure to change the DTMF tone duration using method 1.

Figure 4-2 shows a flowchart of a procedure to change the RTS-CTS delay using method 2.

Figure 4-3 shows a flowchart of a procedure to change the THRESHU value for TONEA using method 3.

Figure 4-4 shows a flowchart of a procedure to read EQM using method 4.

Table 4-1. Interface Memory RAM Addresses

No.	Function	Method	Address (Hex)
1	V.34 Transmitter Speed	1	2E5
	V.34 Receiver Speed	1	2E4
2	V33 Rate Sequence		2C8, 2C9
3	DTMF Tone Duration	2	2DB, 218 (see Note 1)
4	DTMF Interdigit Delay	2	2DC, 219(see Note 1)
5	DTMF Low Band Power Level	2	29C, 29B (see Note 1)
6	DTMF High Band Power Level	2	29E, 29D (see Note 1)
7	Pulse Relay Make Time	1	22C
8	Pulse Relay Break Time	1	21C
9	Pulse Interdigit Delay	2	21B, 21A
10	Calling Tone On Time	2	2D9, 290 (see Note 1)
11	Calling Tone Off Time	2	2DA, 291 (see Note 1)
12	Transmitter Output Level Gain (G) - All Modes	1	3DB, 3DA
	Transmitter Output Level Gain (G) - FSK Modes	3	B57
13	Dual Tone 1 Frequency	2	281, 280 (see Note 1)
14	Dual Tone 2 Frequency	2	283, 282 (see Note 1)
15	Dual Tone 1 Power Level	2	285, 284 (see Note 1)
16	Dual Tone 2 Power Level	2	287, 286 (see Note 1)
17	New Status (NEWS) Masking Registers		
	Masking Register for 01	1	247
	Masking Register for 0A and 0B	2	246, 245
	Masking Register for 0C and 0D	2	244, 243
	Masking Register for 0E and 0F	2	242, 241
	Masking Register for 12 (set bit 7 to enable interrupt)	1	089 (bit 7)
	Masking Register for 14	1	38A
	Masking Register for 16	1	370
	Masking Register for 17	1	371
	Masking Register for 1A and 1B	2	27D, 27C
	Masking Register for Memory Access		
	(Set bit 6 to disable interrupt)	1	089 (bit 6)
22	Signal to Noise Ratio (Measured during Probe)	1 (RO)	11E
23	Low Band Edge Frequency	1 (RO)	11C
	High Band Edge Frequency	1 (RO)	11D
24	CTS OFF-to-ON Response Time (RTS–CTS Delay)	2	203, 202 (see Note 1)
25	Answer Tone Length	2	229, 228 (see Note 1)
26	Silence after Answer Tone Period	2	22B, 22A (see Note 1)
27	Tone Detector A Bandpass Filter Coefficients	3	See Table 4-9
28	Tone Detector B Bandpass Filter Coefficients	3	See Table 4-9
29	Tone Detector C Bandpass Filter Coefficients	3	See Table 4-9
30	RLSD Drop Out Timer	1	270 and 271
31	RLSD Turn-On Threshold (RLSD_ON)	2	135, 134
32	RLSD Turn-Off Threshold (RLSD_OFF)	2	137, 136
	RLSD Threshold Offset	2	139, 138
	RLSD Overwrite Control	1	10D (Bit 2)
	Extended RTH Control	1	10D (Bit 6)
34	Carrier Frequency (TX)	1 (RO)	109 (Bit 0)
	Carrier Frequency (RX)	1 (RO)	211 (Bit 0)

Table 4-1. Interface Memory RAM Addresses (Cont'd)

No.	Function	Method	Address (Hex)
36	AGC Gain Word	4	A00
45	Equalizer Frequency Correction	4	811
46	Eye Quality Monitor (EQM)	4	20C
47	Maximum Period of Valid Ring Signal	1	21F
48	Minimum Period of Valid Ring Signal	1	21E
49	Phase Jitter Frequency	4	80E
50	Phase Jitter Amplitude	4	80D
51	Trellis Mapping (TX)	1 (RO)	375 (Bits 3-4)
52	ITU-T CRC 32 Select	1	0B3
54	Non-linear Encoding (warping) Tx	3	C08 (Bit 10)
55	Non-linear Encoding (warping) Rx	3	C00 (Bit 10)
58	Precoding (TX)	1 (RO)	2FD (Bit 3)
	Precoding (RX)	1 (RO)	052 (Bit 2)
60	V.34 Symbol Rate Value	1	2E3
61	V.34 Baud Rate Mask (BRM)	1	101
62	V.34 Pre-Emphasis Value	4	B44
63	V.34 Pre-Emphasis Override	1	0E6
	V.34 Pre-Emphasis Disable (PREDIS)	1	100 (bit 1)
64	V.34 Transmit Level Deviation Disable (TLDDIS)	1	100 (bit 3)
65	Training (TRN) 4/16-Point Selection	1	100 [bit 7]
68	EQM Above Threshold	1	133
69	ARA-in-RAM Enable	1	3A5 (bit 4)
	EQM Scale Factor (Gain)	3	A29
70	V.21/V.23 CTS Mark Qualify	1	10D (bit 3)
71	V.34 Constellation Size	1	38F (Bit 5)
72	Auto HDLC in Primary Channel	1	3DF (Bit 5)
73	Asymmetric Control Channel Rates Enable	1	3DF (Bit 6)
74	Receive FIFO Trigger Level	1	32C
75	RXFIFO Clear	1	031 (Bit 7)
	TXFIFO Clear	1	031 (Bit 3)
81	V.34 Spectral Parameters Control	1	105
82	V.34 Phase 2 Power Reduction	1	0E2
83	V.34 Phase 2 Guard Tone Level	1	38F (Bit 2)
85	V.34 Data Rate Mask	2	383, 382
86	V.34 Asymmetric Data Rates Enable	1	13F (Bit 6)
87	V.34 Remote Mode Data Rate Capability	2 (RO)	209, 208
88	V.8 Status Registers - See Section 9		
	V.8 Status Register 1	1	301
	V.8 Status Register 2	1	302
	V.8 Status Register 3	1	303
89	V.8 Control Registers - See Section 9		
	V.8 Control Register 1	1	304
	V.8 Control Register 2	1	305
	V.8 Control Register 3	1	306
	V.8 Control Register 4	1	307
	V.8 Control Register 5	1	308
90	Modulation Modes- See Section 9		
	V.17 configuration	1	30D
	V.29 configuration	1	30E
	V.27 configuration	1	30F
	V.23 Full-Duplex configuration	1	312
	V.23 Half-Duplex configuration	1	313
	V.21 configuration	1	314
91	V.8 MaxFrameByteCount- See Section 9	1	31C

Table 4-1. Interface Memory RAM Addresses (Cont'd)

No.	Function	Method	Address (Hex)
92	V.8 Call Functions- See Section 9	1	32A
93	CM/JM/CI Frame - See Section 9		
	SYNC CM/JM/CI	1	32D
	Data Call Function	1	32E
	Modulation 0	1	32F
	Modulation 1	1	330
	Modulation 2	1	331
	Protocol (optional)	1	332
	GSTN (optional)	1	333
	Frame End	1	334
100	Minimum On Time (DTMF)	3	E96
101	Minimum Off Time (DTMF)	3	C96
102	Minimum Cycle Time (DTMF)	3	D96
103	Minimum Dropout Time (DTMF)	3	F96
104	Maximum Speech Energy (DTMF)	3	E95
105	Frequency Deviation, Low Group (DTMF)	3	C94
106	Frequency Deviation, High Group (DTMF)	3	E94
107	Negative Twist Control, TWIST4 (DTMF)	3	D95
108	Positive Twist Control, TWIST8 (DTMF)	3	C95
109	Maximum Energy Hit Time (DTMF)	3	E87
110	DTMF Receiver in FSK Modes	3	C0E (Bit C)
111	Flags2TX	1	2A6
112	Transmitter Compromise Equalizer Coefficients	3	AD0 - AED
113	Number of Taps	3	B47

Notes:

1. High address = MSB of data; low address = LSB of data.
2. The host may access only the X or Y data on any given read cycle, i.e., X and Y data cannot be accessed simultaneously.
3. RO = read-only.

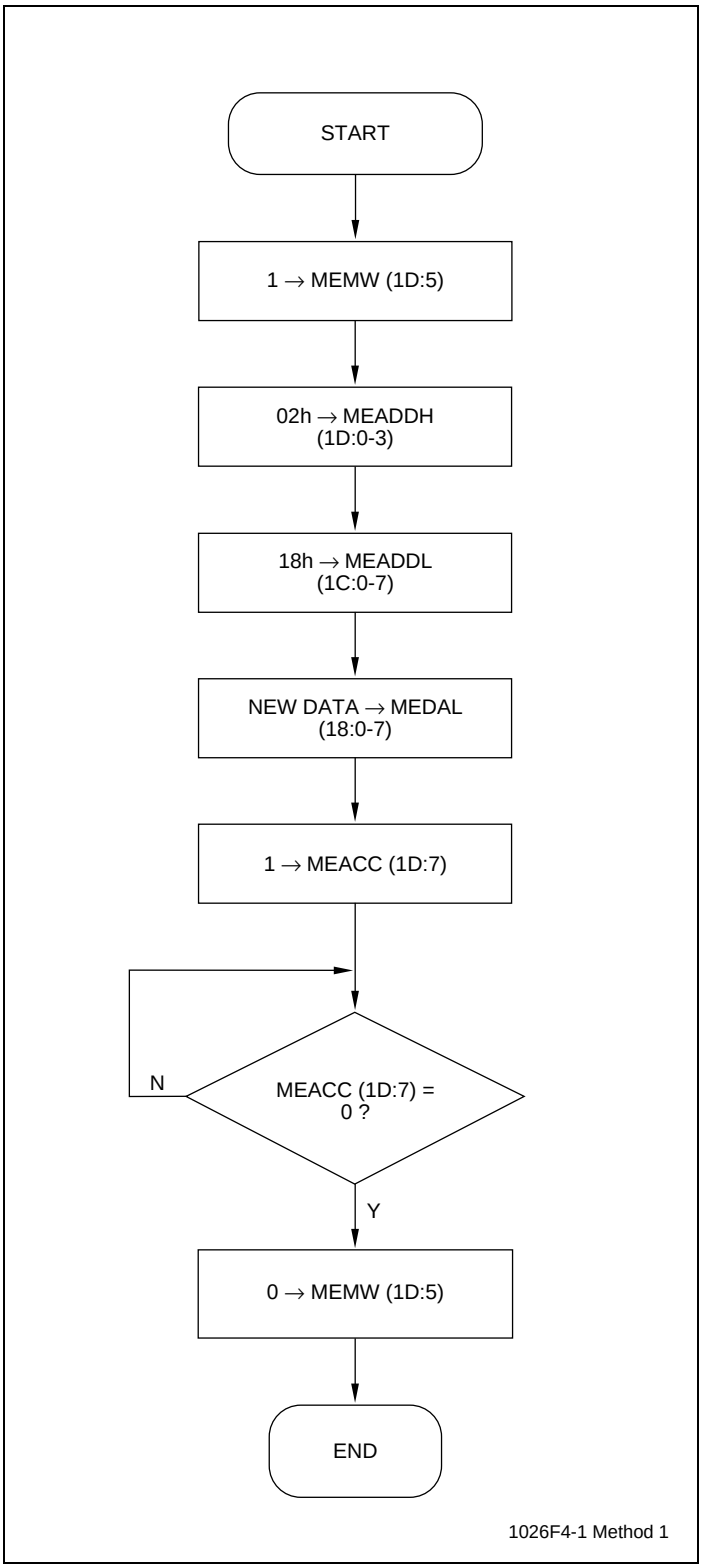

Figure 4-1. Method 1 Example - Changing DTMF Tone Duration (LSB)

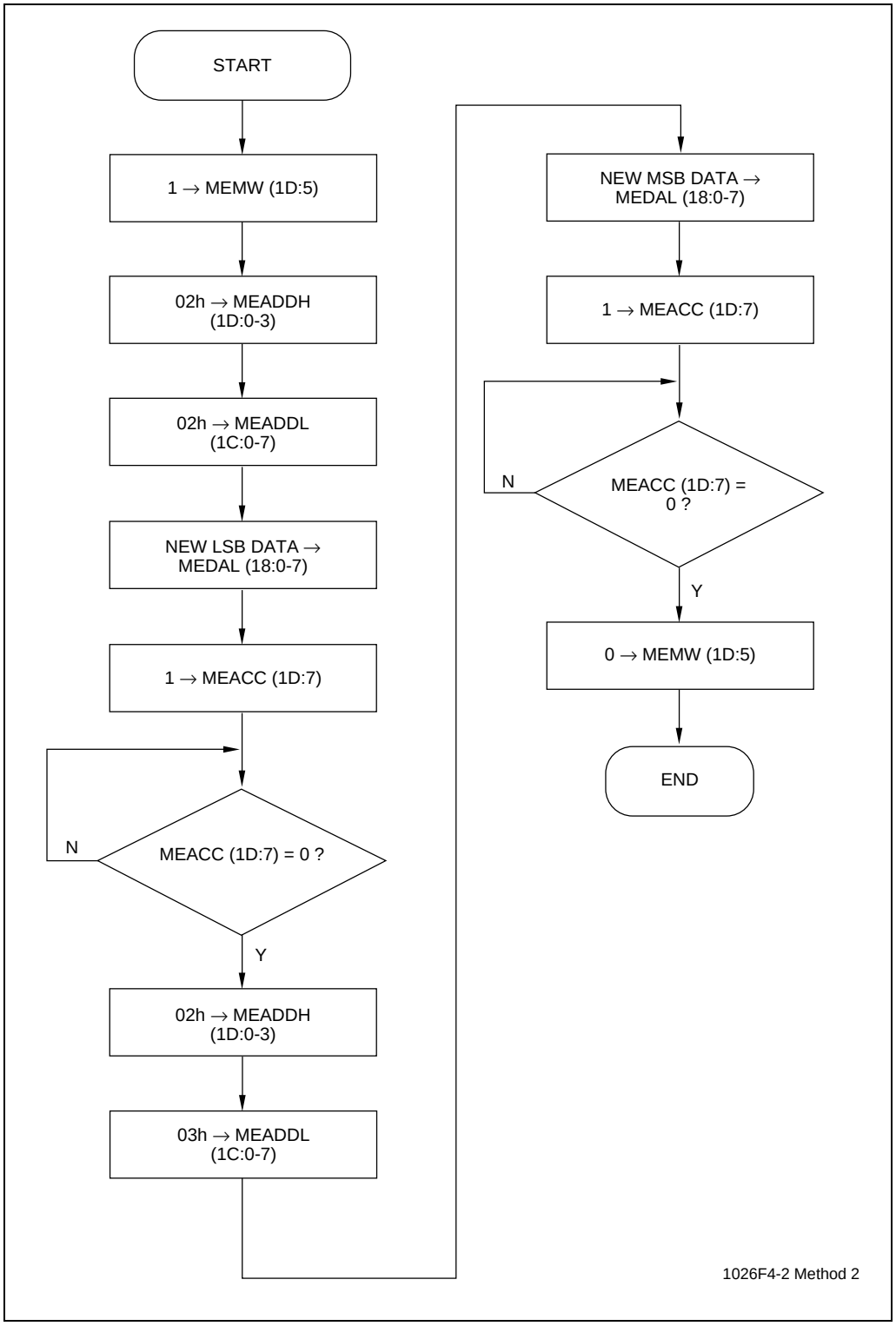

Figure 4-2. Method 2 Example - Changing RTS-CTS Delay

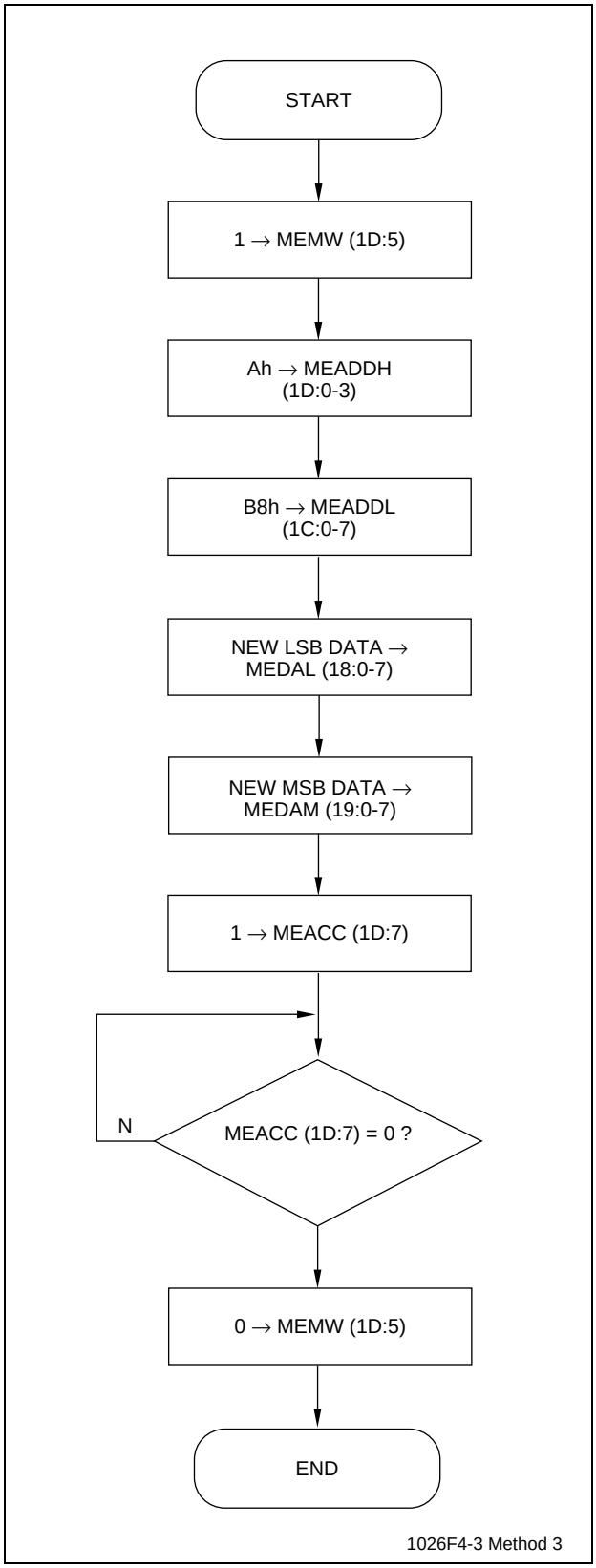

Figure 4-3. Method 3 Example - Changing TONEA THRESHU

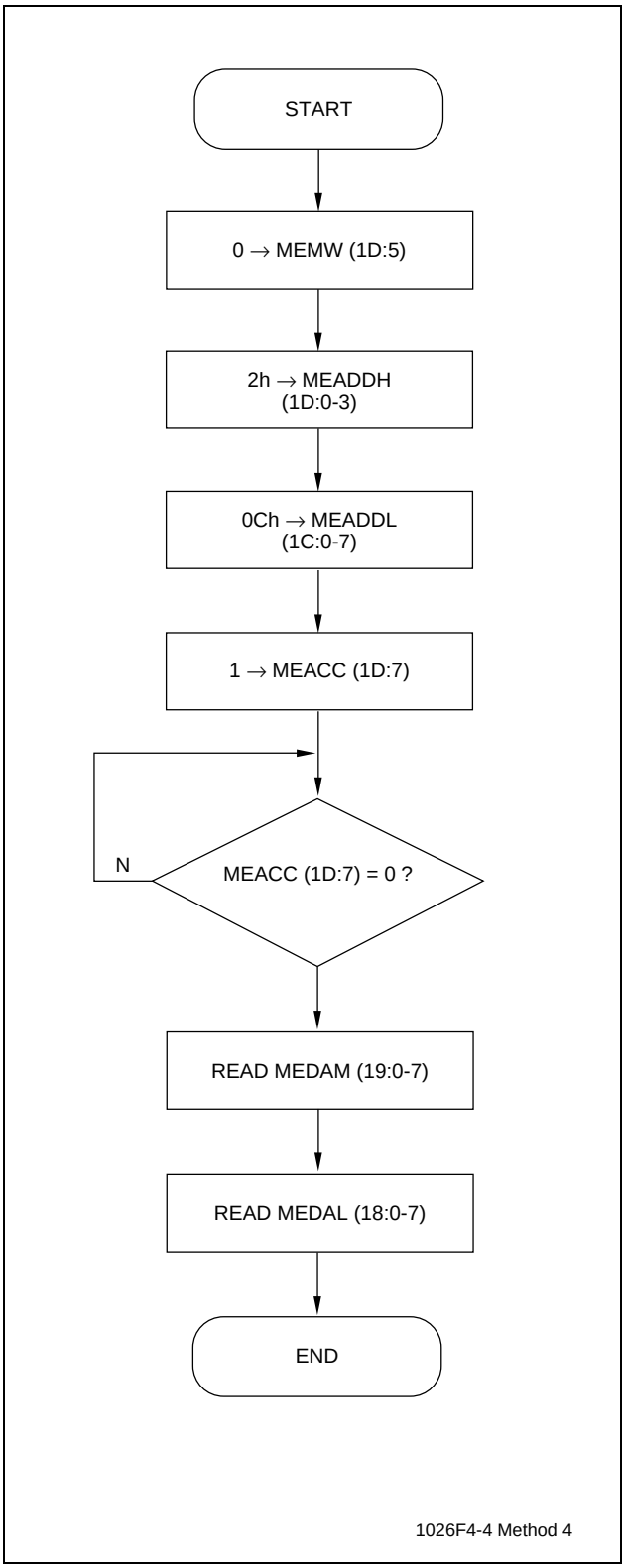

Figure 4-4. Method 4 Example - Reading EQM

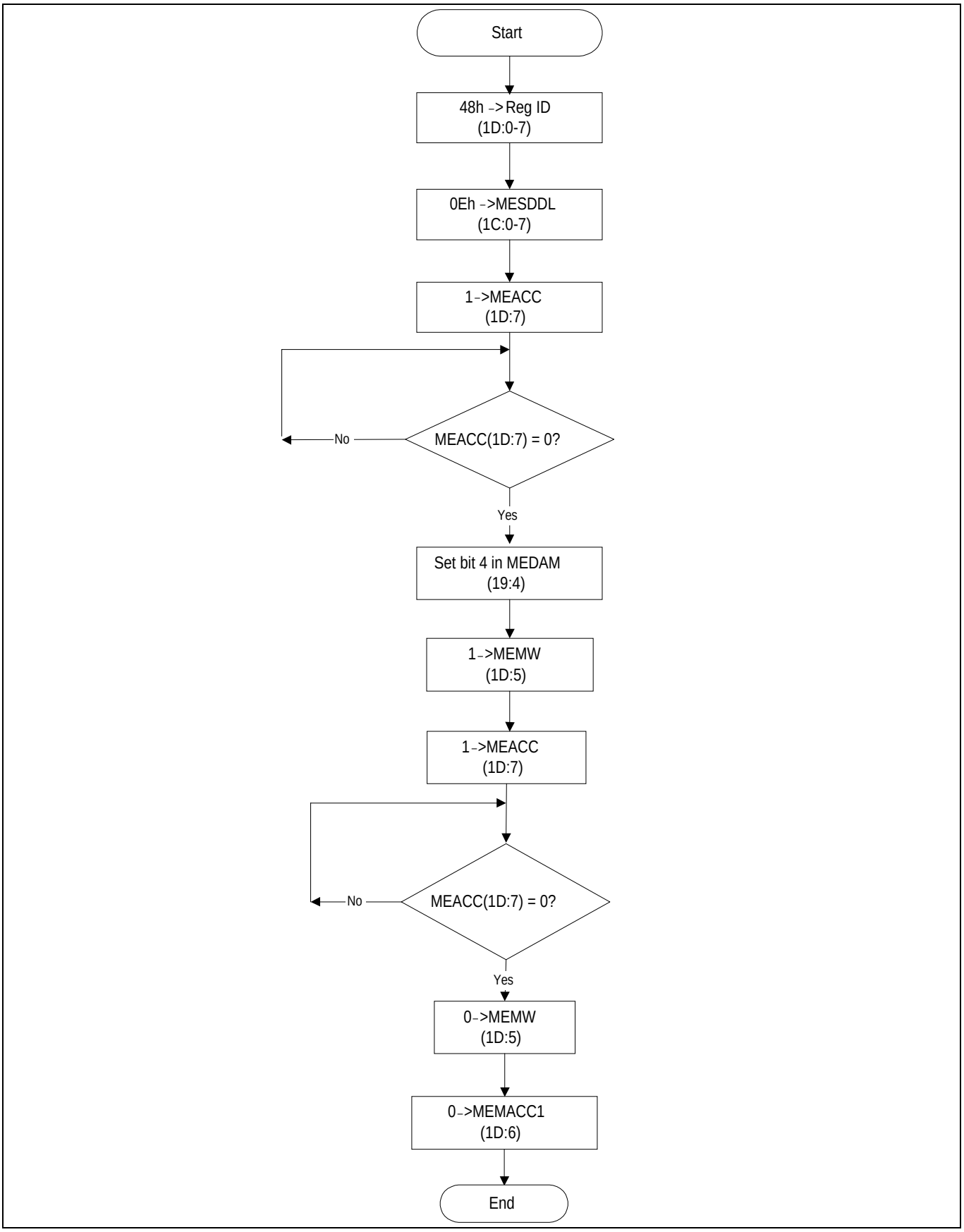

Figure 4-5. Special Access Example - Enable DTMF in FSK Modes

4.4 DSP RAM DATA SCALING

Function 1: V.34 Transmitter Speed **Acc. Method: Addr.: 2E5**
V.34 Receiver Speed **Acc. Method: 1 Addr.: 2E4**

When connected in V.34, the current transmitter and receiver speeds may be read from 2E5 and 2E4, respectively. These locations are updated after each handshake, retrain or rate renegotiation. The speeds are reported as follows:

Speed (kbps)	Value from 2E5 or 2E4	Speed (kbps)	Value from 2E5 or 2E4
33.6	0E	16.8	07
31.2	0D	14.4	06
28.8	0C	12.0	05
26.4	0B	9.6	04
24.0	0A	7.2	03
21.6	09	4.8	02
19.2	08	2.4	01

Function 2: V.33 Rate Sequence **Acc Method: Table 4-1** **Addr. 2C8, 2C9**

V.33 Rate Sequence Bits. ITU-T defines the V.33 rate sequence bits as follows:

4.4.1.1 For B14 = 0:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	0	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on the rate sequence
B4-B6, B10, B12, B13	Not defined
B8	A 1 denotes the ability to receive at 12000 bps
B9	A 1 denotes the ability to receive at 14400 bps

4.4.1.2 For B14 = 1:

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA	0	0	0	0	X	X	X	1	X	X	X	1	X	X	1	1

B0 = MSB; B15 = LSB

Bit	Description
B0-B3, B7, B11, B15	For synchronizing on the rate sequence
B4, B5	A 00 denotes that B6, B10, B12, and B13 define multiplexer configuration selection
B8	A 1 denotes the ability to transmit and receive at 12000 bps
B9	A 1 denotes the ability to transmit and receive at 14400 bps
B6, B10, B12, B13	Multiplexer configuration selection (see the V.33 specification for multiplexer configurations)

The V.33 rate sequence contain undefined codes and/or bits. The user can use these bits to convey information to the remote modem during training (e.g., remote configuration, multiplexer configuration, test mode configuration, etc.).

The 16-bit rate sequence word in the modem's RAM corresponds exactly to the 16-bit rate sequences defined in V.33. The MSB of the word in RAM is B0 of the rate sequence and the LSB is B15 of the rate sequence.

Functions 3-11: Dialing Parameters **Acc. Method: See Below** **Addr.: See Below**

For Functions 3, 4, 7, 8, and 9, the time T (in ms) is calculated as follows:

Equation: $N = T \times 2.4$

Where: N is the decimal value of the hex number written to RAM (1-FFh).

A value of 0000 for the DTMF or calling tone on time will cause the modem to transmit the tone continuously until FFh is written into TBUFFER.

For functions 10 and 11, the time (in ms) is calculated as follows:

Equation: $N = T/10$

For Functions 5 and 6, the DTMF low band or high band power level (P) in dBm is calculated as follows:

Equation: $N = \log^{-1}(P/20) \times 10143$

Where: N is the decimal value of the hex number written to RAM.

Notes:

1. The compromise equalizer is automatically disabled by the transmitter when sending DTMF tones, single tones, or dual tones. The DTMF levels are not affected by the transmit level bits (TLVL). The calling tones, however, are affected by the TLVL bits.
2. Maximum output power = -0.5 dBm.

The dialing parameters and their default values are:

Function	Parameter	Method	Address	Default (Hex)	Default (Dec)
3	DTMF Tone Duration	2	2DB, 218	00DD	92 ms
4	DTMF Interdigit Delay	2	2DC, 219	00AD	72 ms
5	DTMF Low Band Power Level	2	29C, 29B	19C0	– 4.0 dBm
6	DTMF High Band Power Level	2	29E, 29D	2085	– 2.0 dBm
7	Pulse Relay Make Time	1	22C	56	36 ms
8	Pulse Relay Break Time	1	21C	99	64 ms
9	Pulse Interdigit Delay	2	21B, 21A	0708	750 ms
10	Calling Tone On Time	2	2D9, 290	0032	500 ms
11	Calling Tone Off Time	2	2DA, 291	00C8	2 sec

Some DTMF power level values are:

L (dBm)	N (Hex)
–1	2350
–2	1F78
–3	1C0C
–4	1900
–5	1648
–6	13DB

Function 12: **Transmitter Output Level Gain-All Modes** **Acc. Method: 3** **Addr.: 3DB, 3DA**
Transmitter Output Level Gain-FSK Modes **Acc. Method: 3** **Addr.: B57**

Transmitter Output Level Gain-All Modes (Addr. 3DB, 3DA)

The transmitter output level gain constant (G) in dBm is calculated from the following equation:

Equation: $N = \log^{-1} [G/20] \times 16384$

Where: N is the decimal value of the hex number written to RAM.

Range: 0 - 7FFFh (Default = 4000h)

The transmitter output level gain constant directly controls the output level of all configurations. It is used for fine tuning the output level which is controlled by the TLVL bits. Therefore,

Output Level = TLVL Setting + Transmitter Output Gain in dBm

Example gain values are:

G (dBm)	N (Hex)	G (dBm)	N (Hex)
+6	7FB2	-8	197A
+5	71CF	-9	16B5
+4	656E	-10	143D
+3	5A67	-11	1209
+2	5092	-12	1013
+1	47CF	-13	0E53
0	4000	-14	0CC5
–1	390A	-15	0B61
–2	32D6	-16	0A24
–3	2D4E	-17	090A
–4	2861	-18	080E
–5	23FD	-19	072E
-6	2013	-20	0666
-7	1C96	-21	05B4

The MSB goes to address 3DB, while the LSB must be written to 3DA. For example, if TLVL is set for -9 dBm and the required level is -30 dBm, the difference is -21 dBm. Therefore, load address 3DB with 05h, and 3DA with B4h..

The dynamic range of the scale factor is effective from +6 dB down to approximately -60 dB, with a resolution of 0.5E-3 dB.

Setting NEWC to a 1 will put this parameter in force.

Transmitter Output Level Gain-FSK Modes (Addr. B57)

Equation: $N = \log^{-1} [PO/20] \times C$

Where: PO is based on TLVL = 9 and transmit output gain constant (all modes) and A48 = 4000h.

N is the decimal value of the hex number written to RAM.

C = See the following table:

Configuration	CEQ	C (Dec) - Answer	C (Dec) -Originate
V.21	CEQ = 1	9728	10608
	CEQ = 0	8448	8448
Bell 103	CEQ = 1	9072	10496
	CEQ = 0	8704	8352
V.23/1200 TX	CEQ = 1	12800	12800
	CEQ = 0	12544	12544
V.23/75 TX	CEQ = 1	10496	10496
	CEQ = 0	8448	8448

Setting NEWC to a 1 will reset this parameter to the default value.

Function 13: Dual Tone 1 Frequency **Acc. Method: 2** **Addr.: 281, 280**
Function 14: Dual Tone 2 Frequency **Acc. Method: 2** **Addr.: 283, 282**

Frequency F (in Hz) is calculated as follows:

Equation: N = F/0.109863 (Default = 0)

Where: N is the decimal value of the hex number written to RAM.

A single or dual tone is transmitted by writing 80h (single tone) or 83h (dual tone) to the CONF register, programming the tone transmit location in RAM, and then activating RTS. The tone will be transmitted as long as RTS is active.

Example values are:

F (Hz)	N (Hex)	F (Hz)	N (Hex)
400	0E39	2100	4AAB
445	0FD2	2250	5000
600	1555	2400	5555
1200	2AAB	3000	6AAB
1800	4000	3600	8000

Function 15: Dual Tone 1 Power Level **Acc. Method: 2** **Addr.: 285, 284**
Function 16: Dual Tone 2 Power Level **Acc. Method: 2** **Addr.: 287, 286**

Dual tone power level in dBm (PO) is calculated as follows:

Equation: $N = 22304\ [10^{Po/20}]$ (Based on TLVL = 0 and 600 Ω termination.)

Where: N is the decimal value of the hex number written to RAM.

Range: 0 - 7FFFh (Default = 2000h)

Notes:

1. The modem accepts change only when RTS is off.
2. The Transmit Level bits (TLVL) affect output level.
3. Power out = PO + TLVL setting + transmitter output gain constant.

Function 17A: New Status (NEWS) Masking Registers **Acc. Method: See Table 4-1** **Addr.: See Below**
Function 17B: Memory Access Masking Register **Acc. Method: 1** **Addr.: 089 (Bit 6)**

Writing a 1 in the bit location corresponding to the desired bit will cause NEWS to go active when a status change occurs for the selected bit. All bits default to 0 at power-on-reset. Figure 4-6 shows the applicable masking register bits.

In addition, address 089 (bit 6) controls memory access interrupt (set bit 6 to disable interrupt; reset bit 6 to enable interrupt).

Register Address	Bit 7	6	5	4	3	2	1	0	Mask Address (Hex)
1B	EDET	DTDET	OTS	DTMFD	DTMFW				27C
1A	—	—	—	—	DTMFW	—	—	—	27D
17	Secondary Transmit Data Buffer/V.34 Transmit Status (SECTXB)								371
16	Secondary Receive Data Buffer/V.34 Receive Status (SECRXB)								370
14	ABCODE								38A
12	Configuration (CONF)								089, bit 7 = 1
0F	RLSD	FED	CTS	DSR	RI	—	RTSDT	V54DT	241
0E	—	BRKD	—	SPEED					242
0D	P2DET	PNDET	—	—	—	—	TXFNF	—	243
0C	PCOFF	—	—	—	SDET	SNDET	RXFNE	—	244
0B	TONEA	TONEB	TONEC	ATV25	—	—	—	EQMAT	245
0A	PNSUC	FLAGDT	PE	FE	OE	CRCS	FLAGS	SYNCD	246
01	—		—	—	—	TXHF	RXHF	—	247

Figure 4-6. NEWS Masking Registers

Function 22: Signal to Noise Ratio (Measured During Probe) Acc. Method: 1 (RO) Addr.: 11E

Equation: SNR in dB = 1.7(X) - 7

Where X = decimal equivalent of value read in 11Eh.

May be read anytime after SECRXB = 4X. (Recipient modem only.)

Function 23: High Band Edge Frequency Acc. Method: 1 (RO) Addr.: 11D

Equation: Upper -3 dB edge - 37.5(X) + 2400

Where X = decimal equivalent of value read in 11Dh

May be read anytime after SECRXB = 4X. (Recipient modem only.)

Low Band Edge Frequency Acc. Method: 1 (RO) Addr.: 11C

Equation: Lower -3 dB edge - 37.5(X) + 150

Where X = decimal equivalent of value read in 11Ch

May be read anytime after SECRXB = 4X. (Recipient modem only.)

Function 24: CTS OFF-to-ON Response Time (RTS-CTS Delay) Acc. Method: 2 Addr.: 203, 202

Function 24 determines the CTS off-to-on response time in 2-wire half-duplex configurations.

This function can help overcome problems at the V.34 high data rates where there is a period when the receiver has not settled down. This delay is set by loading the required number of symbol rate periods in which to delay the CTS on time in RAM location 202h. The maximum amount of delay is 64 symbol times. Note that symbol times do vary. During the delay time, the transmitter will send marks.

The response time equations and default values are:

Configuration	Equation	Default Value (Hex)	Default Value (Dec)
V.34	N = (Response time x 2.4 ms) –1	0000	0.4 ms
V.21	N = (Response time x 0.298 ms) –1	0098	525 ms
V.23/1200Tx	N = Response time x 1.2 ms	00FC	210 ms
V.23/75Tx	N = Response time x 0.072 ms	0010	235 ms
Where: N is the decimal value of the hex number written to RAM.			

Note: Response time may vary by ± 2 baud times.

Function 25: Answer Tone Length Acc. Method: 2 Addr.: 229, 228

Function 26: Silence After Answer Tone Period Acc. Method: 2 Addr.: 22A 22B

The ITU-T 2100 Hz answer tone length and silence after answer tone are calculated as follows:

Configuration	Equation
V.8, V.21	N = T x 300
V.23/75Tx, V.23/1200Rx	N = T x 75
V.23/1200Tx, V.23/75Rx	N = T x 1200
Where: N is the decimal value of the hex number written to RAM and T is the time is seconds.	

The modem will rewrite the default values when DTR is turned off or the NEWC bit is set.

The end of answer tone transmission may be determined by monitoring address 051, bit 3. This bit will be set to a 1 when the answer has finished and the silence period has commenced. Unless a power-on reset is performed, this bit must be reset by the host if it is to be monitored again on the following connection.

Note: Address 229, 228 lengthens individual phase reversal times in V.8. The answer tone length may be adjusted by increasing or decreasing the number of phase reversals at address 04B. The default value at address 04B is 08h (8 phase reversals). This value may be changed only after DTR is set.

Functions 27 - 29: Tone Detector Bandpass Filter Coefficients **Acc. Method: 3** **Addr.: See Table 4-2**

The implementation of the filters allows user definition of the characteristics of the prefilter and the three tone detectors. Table 4-2 provides the DSP RAM address codes for the filter coefficients. Table 4-3 shows the default values.

Table 4-2. TONEA, TONEB, and TONEC DSP RAM Addresses

	TONEA		TONEB		TONEC		Prefilter	
Parameter	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2	Biquad1	Biquad2
A3	AA1	BA1	AA7	BA7	AAD	BAD	AB2	BB2
A2	AA2	BA2	AA8	BA8	AAE	BAE	AB3	BB3
A1	AA3	BA3	AA9	BA9	AAF	BAF	AB4	BB4
B2	AA4	BA4	AAA	BAA	AB0	BB0	AB5	BB5
B1	AA5	BA5	AAB	BAB	AB1	BB1	AB6	BB6

Table 4-3. TONEA, TONEB, and TONEC Default Values

	TONEA		TONEB		TONEC	
Parameter	Address	Value (Hex)	Address	Value (Hex)	Address	Value (Hex)
LPFBK	BA0	7F30	BA6	7E67	BAC	7F30
LPGAIN	AA0	00CF	AA6	02DF	AAC	00CF
THRESHU	AB8	0880	AB9	2A00	ABA	1600
THRESHL	BB8	0580	BB9	1C00	BBA	0A00

Function 30: RLSD Drop Out Timer **Acc. Method: 1** **Addr.: 270, 271**

V33, V17, V29, V27, and V.21 channel 2

RAM address 270, 271 holds the value for a 16-bit counter which decrements at a baud interval when energy is removed from RXA. When the counter reaches 0000, RLSD turns off. The count down may be observed in RAM addresses 389 (value from address 271) and 388 (value from address 270). The value in address 271 (MSB), 270 (LSB) may be changed anytime after RLSD = 1. The default time may be read in address 271, 270 after RLSD = 1. See Table 1-1 for baud rates of individual modes. By prolonging the RLSD on-off time, the modem can be kept in a freeze mode which can be used to bridge long dropouts. Dropouts of several seconds can be bridged by extending this timer.

Function 31:	**RLSD Turn-On Threshold (RLSD_ON)**	**Acc. Method: 2 Addr.: 135, 134**
Function 32:	**RLSD Turn-Off Threshold (RLSD_OFF)**	**Acc. Method: 2 Addr.: 137, 136**
	RLSD Threshold Offset	**Acc. Method: 2 Addr.: 139, 138**
	RLSD Overwrite Control	**Acc. Method: 1 Addr.: 10D (Bit 2)**
	Extended RTH Control	**Acc. Method: 1 Addr.: 10D (Bit 6)**

A control bit (address 10D, bit 2) enables or disables the over-writing of the RLSD thresholds by the modem's own default threshold table [0 = overwriting enabled (default); 1 = overwriting disabled]. The default state is initialized only by power on or a soft reset.

The RLSD thresholds are loaded into memory locations RLSD_ON and RLSD_OFF. During the Idle mode initialization, the 2-byte value stored in RLSD_ON is used as the RLSD on threshold. When the modem is in Data mode, the 2-byte RLSD_OFF value is used for the RLSD off threshold.

During reset, the respective thresholds are loaded into RLSD_ON and RLSD_OFF as initial values. After reset, the host may then alter these values using the following procedure:

1. Set 10D, bit 2 (to prevent custom values from being overwritten by default values).
2. Load in the custom RLSD values.
3. Set NEWC.

Note: the thresholds can be over-written at any time, but this method ensures that the first connection after a NEWC uses the correct value of ON threshold.

Extended RLSD Threshold Selection;

The Extended RTH bit (XRTH) (address 10D, bit 6) controls the reduction of RLSD thresholds by approximately 5 dBm [0 = disables reduction (default); 1 = enables reduction]. If XRTH is a 1, RTH must be reset to 0. This extended RLSD threshold method affects all configurations while preserving the hysteresis.

The amount of threshold reduction (offset) can be controlled manually by the host writing a 16-bit offset value into address 139, 138. For example, this offset is useful for compensating for any loss or gain that may be introduced by the DAA/hybrid used. Note that if a negative offset is wanted, then the twos complement number should be entered. The maximum amount of offset that can safely be subtracted is 900 (F700h, 2s complement).

Function 34: Carrier Frequency (TX) **Acc. Method: 1 (RO)** **Addr.: 109 (Bit 0)**
Carrier Frequency (RX) **Acc. Method: 1 (RO)** **Addr.: 211 (Bit 0)**

Range: 1 = high frequency
0 = low frequency

Not applicable to 3429 symbol rate - only one frequency specified. May be read anytime after SECRXB = 4Xh.

Function 36: AGC Gain Word **Acc. Method: 4** **Addr.: A00**

Function 36 is useful for determining the receive level (RL) at the Receive Analog (RXA) input. The number in RAM is related to the receive level as follows:

Configuration	Equation
V.34, V.33, V.17, V.29, V.27	RL = N/682.7 - 52 dB
V.23/1200	RL = N/682.7 - 48 dB
V.21, V.23/75	RL = N/682.7 - 54 dB
Where: N is the decimal value of the hex number read from RAM.	

This formula is valid only if the receive level is above the RLSD off-to-on threshold.

Function 46: Eye Quality Monitor **Acc. Method: 4** **Addr.: 20C**

The EQM value may be read from this location. (See Section 4.6.1 for more information.)

Function 47: Maximum Period of Valid Ring Signal **Acc. Method: 1** **Addr.: 21F**

Function 48: Minimum Period of Valid Ring Signal **Acc. Method: 1** **Addr.: 21E**

The ring detector measures the period of pulses on the ring detect input and determines whether the pulses are within the frequency range specified by the Maximum Period of Valid Ring Signal and Minimum Period of Valid Ring Signal functions. Since maximum period corresponds to minimum frequency, the formula for calculating these functions is given in terms of frequency.

Frequency F (in Hz) is calculated as follows:

Equation: N = 2400/F

Where: N is the decimal value of the hex number written to RAM (05h-FFh).

Default: The default values are:

Function	Parameter	Method	Address	Default (Hex)	Default (Dec)
47	Maximum Period of Valid Ring Signal	1	21F	A0	15 Hz
48	Minimum Period of Valid Ring Signal	1	21E	23	68 Hz

Note: Writing 00 to Function 48 will cause the RI bit state and ~RI output pin level to follow the RINGD input pin level.

Function 49: Phase Jitter Frequency **Acc. Method: 4** **Addr.: 80E**

The phase jitter frequency estimate is available in V.34 mode only. The phase jitter amplitude must be greater than approximately 6 degrees with a minimum frequency of 10 Hz in order for the modem to lock on and track the jitter.

Equation: $F = N*\text{Symbol Rate}/2^{16}$

Where: F is the frequency in Hz.
N is the decimal equivalent of the hex number read from RAM.
Symbol Rate = 2400, 2800, 3000, 3200, or 3429.

Function 50: Phase Jitter Amplitude **Acc. Method: 4** **Addr.: 80D**

The phase jitter amplitude estimate is available in V.34 mode only. The phase jitter amplitude must be greater than approximately 6 degrees with a minimum frequency of 10 Hz in order for the modem to lock on and track the jitter.

Equation: AP = N/90

Where: AP is the amplitude in degrees.

N is the decimal equivalent (absolute value) of the hex number read from RAM

Function 51: Trellis Mapping (TX) **Acc. Method: 1 (RO)** **Addr.: 375 (Bit 3-4)**

Range: 00 = 16-4D

01 = 32-4D

11 = 64-4D

Receiver always uses 16-4D. May be read anytime after RLSD = 1.

Function 52: ITU-T CRC 32 **Acc. Method: 1** **Addr.: 0B3**

The type of cyclic redundancy check (CRC) generation and detection can be selected by writing to address 0B3, bit 0 [0 = ITU-T CRC 32; 1 = ITU-T CRC 16 (default)].

Function 54: Non-Linear Encoding (Warping) Tx **Acc. Method: 3 (RO)** **Addr.: C08 (Bit A)**

Function 55: Non-Linear Encoding (Warping) Rx **Acc. Method: 3 (RO)** **Addr.: C00 (Bit A)**

Function 58: Precoding (TX) **Acc. Method: 1 (RO)** **Addr.: 2FD (Bit 3)**
Precoding (RX) **Acc. Method: 1 (RO)** **Addr.: 052 (Bit 2)**

Range: 1 = on

0 = off

May be read anytime after RLSD = 1.

Function 59: Shaping (TX) **Acc. Method: 3 (RO)** **Addr.: A49 (Bit 15)**
Shaping (RX) **Acc. Method: 3 (RO)** **Addr.: 9F8 (Bit 15)**

Range: 1 = on

0 = off

May be read anytime after RLSD = 1.

Function 60: Selected Symbol Rate **Acc. Method: 1 (RO)** **Addr.: 2E3**

0 = 2400,

2 = 2800,

3 = 3000,

4 = 3200,

5 = 3429

May be read anytime after SECRXB = 4X

Function 61: V.34 Baud Rate Mask (BRM) **Acc. Method: 1** **Addr.: 101**

During the start-up handshake, the modem probes the communication channel and determines the available bandwidth. This information helps establish the common symbol rate between the modems. The following data rate ranges are available for a selected symbol rate:

Symbol Rate (baud)	Highest Possible V.34 Data Rate (bps)
2400	21600
2800	24000
3000	26400
3200	31200
3429	33600

If line conditions cannot support the higher symbol rates, the modem automatically reduces the data rate to match the allowable symbol rate.

The host can control the symbol rate negotiation process via the Baud Mask Register (BMR), located at address 101. By either setting or resetting one or more of five bits in the BMR, the host can specify if a particular symbol rate is to be

supported. In Loop 3 (L3ACT = 1), the baud rate may be selected by writing the desired symbol rate value (0, 2, 3, 4, or 5) to address 2E3 anytime prior to establishing the loopback. The default value is 4 for 3200 baud. The symbol rates and the corresponding bit positions are:

Symbol Rate (baud)	Symbol Rate Value (Addr. 2E3)	Baud Mask Register (BMR) Enable Bit Position (Addr. 101)
2400	0	0
Reserved	1	1*
2800	2	2
3000	3	3
3200	4	4
3429	5	5
* Bit 1 must always be a 0.		

When the modem determines, from the bandwidth, the maximum supportable symbol rate, the modem will enable all symbol rates below that maximum value. For example, if the line probe indicates that the bandwidth is adequate to support 3000 baud, then 2800 and 2400 baud will also be supported. This selection of symbol rates is, however, dependent upon the contents of the BMR. Again, for the same example, if a host does not want to support 2800 baud, the host must reset bit 2 of the BMR. If both modems do not agree during probing, e.g., the originate modem chooses 3000 baud and the answer modem chooses 2800 baud, then the highest common rate will be 2400 baud. In the event there is no common rate, the modems will default to 2400 baud.

The symbol rate chosen may be read from address 2E3 after the negotiation is complete. A value of 10h, for example, would indicate a symbol rate of 3200 baud.

Function 62: Selected Pre-emphasis **Acc. Method: 3 (RO)** **Addr.: B44**

A hex number 0-A. Indicates the V.34 pre-emphasis filter 0-A as defined in the ITU V.34 specification.

May be read anytime after SECRXB = 4X)

Function 63: V.34 Pre-Emphasis Filter Override Number **Acc. Method: 1** **Addr.: 0E6**
V.34 Emphasis Disable **Acc. Method: 1** **Addr.: 100 (Bit 1)**

For V.34, there are only 11 pre-emphasis filters defined, each matching the templates defined in ITU-T V.34 (Figure 1 and 2).

V.34	
Pre-emphasis Filter Suggestion Number	**Amount of Upper Band Edge Attenuation Compensated (dB)**
0	See ITU-T V.34, Figures 1 and 2.
1	
2	
3	
4	
5	
6	
7	
8	
9	
A	

The pre-emphasis filter selected can be read from the V.34 Pre-Emphasis Filter Number (address B44).

The pre-emphasis negotiation can be ignored by setting address 100, bit 1, Pre-emphasis Disable (PREDIS). This bit does not stop the measurement or the transmission of the suggested pre-emphasis filter, but rather causes the receiver to ignore the suggestion.

Pre-emphasis can also be controlled by using the CEQ bit in the modem interface memory. If this bit is reset, any selected pre-emphasis or transmit compromise filter will be ignored. In this way, the host can control pre-emphasis by

setting/resetting CEQ. However, if the host wishes to use a custom compromise filter, then by using the PREDIS bit, the suggested filter will be ignored and the host's custom defined compromise filter will be used.

The procedure to manually select one of the pre-emphasis filters is:

1. Set PREDIS (address 100, bit 1) to override negotiation.
2. Load the Pre-Emphasis Filter Over-Ride Number (address 0E6) with the Pre-emphasis Filter Suggestion Number from the table above.
3. Ensure that CEQ is on.

Function 64: V.34 Transmit Level Deviation Disable **Acc. Method: 1** **Addr.: 100 (Bit 3)**

During line probing, the modem measures the receive level of the line signal. If that receive level is high enough, the modem suggests that the remote modem reduce its own transmit level in order to improve signal-dependent noise performance.

For V.34, The transmit level power drop does not use receive level alone. Decision is also based on improved noise and harmonic distortion criteria.

To force the modem to ignore the suggested transmit level reduction, set the Transmit Level Deviation Disable (TLDDIS) (address 100, bit 3) to a 1.

Function 65: Training (TRN) 4/16-Point Selection **Acc. Method: 1** **Addr.: 100[bit 7]**

Range: 1 = 4-point

0 =16-point (Default)

Both automatic (by the modem) and manual (by the host) selection of the number of training points is available. Bit 3C1[4] is used to enable forced N-point training mode. To select 4 point, then set bit 100[7] otherwise 16 point mode is used. If 3C1[4] is reset the modem uses an automatic selection algorithm to select either 4 point or 16 point training depending upon certain line conditions. The Threshold for determining the point at which the modem selects either 4 point or 16 point is programmable and is located at 2CD in RAM. The default value is 13h. Which represents a SNR/SHR of approximately 24 dB.

Function 68: EQM Threshold **Acc. Method: 1** **Addr.: 133**

The EQM threshold can be set at this address. When the high byte of the EQM reading (address 20D) goes above the EQM Threshold, the modem will assert the EQMAT bit (register 0B, bit 1). The host can set up a NEWS interrupt to monitor changes to this bit (see EQMAT in Function 17). The default value of EQM Threshold is 30h and is written at POR and is unaffected by NEWC. The modem does NOT reset the EQMAT bit; the host must reset the EQMAT bit.

Function 69: ARA-in RAM Enable **Acc. Method: 1** **Addr.: 3A5 (Bit 4)**
EQM Scale Factor (Gain) **Acc. Method: 3** **Addr.: A29**

The automatic rate adaptation (ARA) algorithm adjusts the data rate based on the level of EQM. The algorithm is used for initial train ARA is enabled by setting the EARC bit (15:0), which defaults off.

Upon initial train and retrain, the EQM is checked towards the end of the training, just before the rate negotiation. The 4-point EQM is compared against a table of values representing the necessary levels to achieve the corresponding data rates with an EQM of around 2000h. Once the maximum achievable rate is determined, the CONF register is changed to reflect the estimate, and is then used to suggest a data rate in the following negotiations.

Function 70: V.21/V.23 CTS Mark Qualify **Acc Method: 1** **Address: 10D (Bit 3)**

In V.21/V.23 configurations, CTS turn-on qualifying time can be controlled by writing to address 10D, bit 3 [0 = no qualifying time after Mark (default); 1 = qualifying time of 45 ±5 ms after Mark]. This bit is unaffected by the action of NEWC.

Function 71: V.34 Constellation Size **Acc. Method: 1** **Addr.: 38F (Bit 5)**

Range: 1 = 1664 points (up to 33.6 kbps user data rate)

0 = xxx points (up to 28.8 kbps user data rate)

Function 72: Auto HDLC in Primary Channel **Acc. Method: 1** **Addr.: 3DF (Bit 5)**

Range: 1 = on

0 = off

When set to on by the host, the modem will automatically be in HDLC mode during primary channel.

Function 73: Asymmetric Control Channel Rates Enable **Acc. Method: 1** **Addr.: 3DF (Bit 6)**

Range: 1 = on

0 = off

When set to on by the host, the modem will allow asymmetric control channel rates if the other modem also has bit 50 of MPh set.

Function 74: Receive FIFO Trigger Level **Acc Method: 1** **Address: 32C**

Details of using the FIFO are given in Section 5.2.

The trigger level of the RX FIFO can be controlled by writing to address 32C. The default value is CBh which gives a trigger level of 14 bytes and a time-out of 17 clock cycles.

Bits 6-7: Trigger Level. Selects the trigger level in the 16-byte RX FIFO. For example, setting bits 7 and 6 to 11 selects a trigger level of 14 bytes. That is, RDBF will not become asserted until the receive FIFO is 14 bytes full and the time-out delay has not elapsed (see below).

B7	B6	Trigger Level (No. of Bytes)
0	0	Trigger level = 1
0	1	Trigger level = 4
1	0	Trigger level = 8
1	1	Trigger level = 14

Bit 5: Must be 0.

Bits 2-4: Time-out Delay. Selects the length of idle time that will cause RDBF to be asserted when the RX FIFO is not empty. Idle time is the length of time that elapses without the modem data pump writing into the RX FIFO or the host reading data from the RX FIFO. This feature prevents data from being "held up" in the RX FIFO.

B4	B3	B2	Idle Time (In Bit Times)
0	0	0	9 bit times
0	0	1	13 bit times
0	1	0	17 bit times
0	1	1	21 bit times
1	0	0	25 bit times
1	0	1	29 bit times
1	1	0	33 bit times
1	1	1	37 bit times

Bit 1: Idle Time Time-out Enable. 1 = the time-out enabled; 0 = time out disabled. When Time out is disabled (0), RDBF will be asserted only when the RX FIFO threshold is reached.

Bit 0: Not Used.

RX FIFO Error Status Bits

The RX FIFO includes five error status bits: BRKD (register 0E, bit 6), SYNCD (register 0A, bit 1), RXP (register 01, bit 0), FE (register 0A, bit 4), and PE (register 0A, bit 5). SYNCD is used for 7E flag detection in HDLC mode only and BRKD indicates that an asynchronous break has been received. FE indicates a framing error in asynchronous mode or an abort condition in HDLC mode. PE indicates an asynchronous parity error or a CRC error in HDLC mode. RXP indicates the received parity bit in 8-bit asynchronous stuff parity mode.

IMPORTANT: The host must read the status bits prior to reading the byte from RBUFFER. Note that this is the opposite of how it should be done using the RC96DPL/RC144DPL or RC96DPi/RC144DPi.)

Also, there are two status bits (RXHF and RXFNE) that the host can use to monitor the RX FIFO operation. RXHF (register 01, bit 1) indicates when the receive FIFO is half full and RXFNE (register 0C, bit 1) is set whenever the RX FIFO has data in it.

Function 75: RXFIFO Clear **Acc. Method: 1** **Addr.: 031 (Bit 7)**
TXFIFO Clear **Acc. Method: 1** **Addr.: 031 (Bit 3)**

When set to one by the host, it will clear the respective FIFO.

Function 81: V.34 Spectral Parameters Control **Acc Method: 1** **Address: 105**

The host can control some of the spectral parameters that the transmitter uses for cases where the local PTT has regulations governing transmission. These control bits can usually be used in their default state and the host need only alter them if required to meet PTT approval.

Bit 7: Transmitter Enable for the Low Carrier Frequency for 3200 Baud. When set, the transmitter is allowed to use the low carrier frequency for 3200 baud.

Bit 6: Transmitter Enable for the High Carrier Frequency for 3200 Baud. When set, the transmitter is allowed to use the high carrier frequency for 3200 baud.

Bit 5: Transmitter Enable for the Low Carrier Frequency for 3000 Baud. When set, the transmitter is allowed to use the low carrier frequency for 3000 baud.

Bit 4: Transmitter Enable for the High Carrier Frequency for 3000 Baud. When set, the transmitter is allowed to use the high carrier frequency for 3000 baud.

Bit 0-3: Reserved. Do not alter the contents.

Function 82: V.34 Phase 2 Power Reduction **Acc Method: 1 (RO)** **Address: 0E2**

In V.34 mode, the modem supports the reduction in transmit power if instructed by the remote modem during the start-up sequence. The amount of power drop from the nominal is 0 to 14 dB. The TLDDIS bit (at location 100 bit 3, see Function 64) enables the local modem to implement the amount of power drop being suggested by the remote modem or to ignore it and not drop the level at all. The Transmit level Deviation Bias (Function 65) also applies to V.34. Function 82 specifies the amount of power drop in dB after Phase 2.

Function 83: V.34 Phase 2 Guard Tone Level **Acc. Method: 1** **Addr.: 38F (Bit 2)**

Range: 1 = Nominal Power

0 = -7 dB of Nominal Power (Default)

The ability to select whether the 1800 Hz guard tone transmitted during phase 2 of the startup sequence is either -7 dB of nominal power or at nominal power.

Function 85: V.34 Data Rate Mask **Acc Method: 2** **Address: 383, 382**

The V.34 data rate masks occupy two bytes in RAM. Locations 382 and 383 represent the lower byte and the upper byte of the mask, respectively (Table 4-4). The bits in the mask represent the enabling of a particular data rate if set or disabled if reset. The definition of the bits are data rate 2400 is at bit 0 (i.e., the LSB of address 382), 4800 is at bit 1, 7200 at bit 2 and so on up to 33600 bps (in 2400 bps increments) which is bit 13 of the mask (or bit 5 of address 383. Bits 14-15 are reserved for future use.

Table 4-4. V.34 Rate Sequence Mask Bit Assignments

Data Rate	V.34 Data Rate Mask-MSB (address 383)								V.34 Data Rate Mask-LSB (address 382)							
(bps)	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
2400	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	1
4800	-	-	X	X	X	X	X	X	X	X	X	X	X	X	1	X
7200	-	-	X	X	X	X	X	X	X	X	X	X	X	1	X	X
9600	-	-	X	X	X	X	X	X	X	X	X	X	1	X	X	X
12000	-	-	X	X	X	X	X	X	X	X	X	1	X	X	X	X
14400	-	-	X	X	X	X	X	X	X	X	1	X	X	X	X	X
16800	-	-	X	X	X	X	X	X	X	1	X	X	X	X	X	X
19200	-	-	X	X	X	X	X	X	1	X	X	X	X	X	X	X
21600	-	-	X	X	X	X	X	1	X	X	X	X	X	X	X	X
24000	-	-	X	X	X	X	1	X	X	X	X	X	X	X	X	X
26400	-	-	X	X	X	1	X	X	X	X	X	X	X	X	X	X
28800	-	-	X	X	1	X	X	X	X	X	X	X	X	X	X	X
31200	-	-	X	1	X	X	X	X	X	X	X	X	X	X	X	X
33600	-	-	1	X	X	X	X	X	X	X	X	X	X	X	X	X

Function 87: V.34 Remote Modem Data Rate Capability **Acc Method: 2** **Address: 209, 208**

The data rate capability of the remote modem is reflected in a binary sequence transmitted by the remote modem during Phase 4 of the handshake. This 12-bit received sequence is stored in locations 208 and 209 (Table 4-5). The definition of this field is the same as that described for the V.34 Data Rate Mask (Function 85). This information is valid after RLSD is

ON. The received V.34 rate sequence indicates the remote modem's true speed capabilities as it is masked only by the remote mask sequence register and not by the remote ARA function (EARC bit = 1). For example, the modem may connect at 24000 bps by request of the remote modem's ARA, yet the received rate sequence may indicate that the remote modem can support 28800 bps. This information may be used for fall forward decisions.

Table 4-5. V.34 Remote Mode Data Rate Capability Bit Assignments

Data Rate	V.34 Remote Mode Data Rate Capability -MSB (Address 209)								V.34 Remote Mode Data Rate Capability-LSB (Address 208)							
(bps)	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
2400	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	1
4800	-	-	X	X	X	X	X	X	X	X	X	X	X	X	1	X
7200	-	-	X	X	X	X	X	X	X	X	X	X	X	1	X	X
9600	-	-	X	X	X	X	X	X	X	X	X	X	1	X	X	X
12000	-	-	X	X	X	X	X	X	X	X	X	1	X	X	X	X
14400	-	-	X	X	X	X	X	X	X	X	1	X	X	X	X	X
16800	-	-	X	X	X	X	X	X	X	1	X	X	X	X	X	X
19200	-	-	X	X	X	X	X	X	1	X	X	X	X	X	X	X
21600	-	-	X	X	X	X	X	1	X	X	X	X	X	X	X	X
24000	-	-	X	X	X	X	1	X	X	X	X	X	X	X	X	X
26400	-	-	X	X	X	1	X	X	X	X	X	X	X	X	X	X
28800	-	-	X	X	1	X	X	X	X	X	X	X	X	X	X	X
31200	-	-	X	1	X	X	X	X	X	X	X	X	X	X	X	X
33600	-	-	1	X	X	X	X	X	X	X	X	X	X	X	X	X

Function 88: V.8 Status Registers - See Section 7.

Function 89: V.8 Control Registers - See Section 7.

Function 90: Modulation Modes- See Section 7.

Function 91: V.8 MaxFrameByteCount- See Section 7.

Function 92: V.8 Call Functions- See Section 7.

Function 93: CM Frame - - See Section 7.

Function 100: Minimum On Time (DTMF) Acc Method: 3 Address: E96

The on-time is defined as the minimum period of time of the DTMF signal beginning when the signal is detected and ending when the energy is below the turn-off threshold. The on-time parameter cannot be set below 20 ms (0000h). The default on-time parameter is set for 40.0 ±1 ms. The on-time will vary with signal level. To increase or decrease the on-time parameter value, convert the increase/decrease into hexadecimal and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Minimum On Time ± [(Increase/Decrease)Sample Rate]h

Default: 48h

Function 101 Minimum Off Time (DTMF) Acc Method: 3 Address: C96

The minimum off time is defined as the minimum period of time of the DTMF signal beginning when the energy falls below the turn-off threshold and ending when a gain hit is detected. The off-time parameter is equal to the desired minimum off-time minus the drop out time. The default off time is set for 40.0 ± 1 ms with a default dropout time parameter of 5.0 ms. To increase or decrease the off-time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Minimum Off Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

Default: EEh

Function 102: Minimum Cycle Time (DTMF) Acc Method: 3 Address: D96

The minimum cycle time is defined as the minimum period of the DTMF signal beginning when the signal is detected and ending when the next signal begins. The cycle time parameter is equal to the desired minimum cycle-time minus the dropout time. The default cycle time parameter is set for 93.0 ±1 ms with a default drop out time parameter of 5.0 ms. To increase or decrease the cycle time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Minimum Cycle Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

Default: 189h

Function 103: Minimum Dropout Time (DTMF) Acc Method: Address: F96

The minimum dropout time is defined as the maximum period of the DTMF signal beginning when the signal energy drops below the turn-off threshold and ending when the signal energy returns that is considered to be part of the on time. The default dropout time parameter is set to 5.0 ms.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: [(Desired time)Sample Rate]h

Default: 1Fh

Function 104: Maximum Speech Energy (DTMF) Acc Method: 3 Address: E95

This parameter specifies the maximum relative speech energy that may be detected and still receive DTMF signals. The speech energy is measured in the frequency region of second or third harmonics of the DTMF tones. To disable the speech energy detector, set this parameter to its full scale positive value (7FFFh). Decreasing the value of this parameter may degrade signal-to-noise ratio (SNR) performance, but may reduce false settings of status bit EDET due to speech signals. To increase or decrease the maximum speech energy parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Maximum Speech Energy ± (Increase/Decrease)h

Default: 519h

Function 105: Frequency Deviation, Low Group (DTMF) Acc Method: 3 Address: C94

This parameter controls the acceptable frequency range for the low group DTMF tones (697, 770, 852, and 941 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Frequency Deviation ±(Increase/Decrease)h

Default: 421h

Function 106: Frequency Deviation, High Group (DTMF) Acc Method: 3 Address: E94

This parameter controls the acceptable frequency range for the high group DTMF tones (1209, 1336, 1477, and 1633 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Frequency Deviation ±(Increase/Decrease)h

Default: 3A8h

Function 107: Negative Twist Control, TWIST4 (DTMF) Acc Method: 3 Address: D95

This parameter controls the acceptable negative twist for the DTMF signals. Decreasing this parameter increases the acceptable negative twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Negative Twist ±(Increase/Decrease)h

Default: 18CEh

Function 108: Positive Twist Control, TWIST8 (DTMF) Acc Method: 3 Address: C95

This parameter controls the acceptable positive twist for the DTMF signals. Decreasing this parameter increases the acceptable positive twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Positive Twist ±(Increase/Decrease)h

Default: 1B2Dh

Function 109: Maximum Energy Hit Time (DTMF) Acc Method: 3 Address: E87

This parameter represents the duration of an allowed energy impulse during the off time measurement. The default value of 0000h means no gain hits will be tolerated during the off time.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: [(Desired Time)(Sample Rate)]h

Default: 0h

Function 110: DTMF Receiver in FSK Modes Acc. Method: 3 Addr.: C0E(Bit 12)

Range: 1 = Enabled **C0C (Bits 15, 14)**

0 = Disabled

To operate the DTMF receiver, the host must set bit 15 in $C0C to initialize the RAM and then set 12 in $C0E to enable the DTMF receiver; the sequence must be as written. Note that bit 14 in $C0C controls the selection of the appropriate filter coefficients for the 7200 Hz or 9600 Hz sample rate. When bit 14 in $C0C is set, 9600 Hz parameters are loaded, otherwise 7200 Hz parameters are loaded.

DTMF reception is not enabled by default in V.8 or V.21 Channel 2 modes. To run the DTMF receiver in V.8 the host must set bits 15 and 14 in $C0E, then set bit 12 in $C0E. Similarly, for V.21 Channel 2, the host must set bit 15 in $C0C, then set bit 12 in $C0E.

Notes: 1. To detect the next digit during ANSam, set the $C0C [15, 14] to 1 to initialize the DTMF receiver.

2. For $Cxx address space access, see section 4.2.

Function 111: Flags2TX Acc. Method: 1 Addr.: 2A6

The minimum number of HDLC flags to transmit between HDLC Frames.

Range: 0-127

Default: 0 for 1 flag

This function does not effect the number of frames sent before the first HDLC frame in a new mode.

Function 112: Transmitter Compromise Equalizer Coefficients **Acc. Method: 3** **Addr.: AD0-AED**

Function 113: Number of Taps **Acc. Method: 3** **Addr.: B47**

The transmitter compromise equalizer can be programmed by the host in modes other than V.34 or FSK. The equalizer is a 25-tap finite impulse response (FIR) digital filter. The first tap is at address AED and the last tap is at AD0. The sampling rate for the filter is 7200 Hz. New coefficients should be loaded while the modem is in idle mode before turning on DTR. The coefficients have to be loaded only once. They are re-initialized to the default values only if a POR occurs. The user should ensure that the overall gain of any filter designed is 1. Set NEWC after new taps have been loaded.

4.5 SOFTWARE INTERFACE CONSIDERATIONS

4.5.1 Interrupt Request Handling

DSP interface memory registers 00, 10, 1E, and 1F have unique hardware connections to the interrupt logic. Register 00 is the Receive Buffer (RBUFFER) and register 10 is the Transmit Buffer (TBUFFER). Registers 1E and 1F hold interrupt flag, interrupt enable, and interrupt active bits. When a condition occurs that satisfies an interrupt criteria, the corresponding interrupt flag bit is set. This interrupt flag can be reported to the host either by the host polling the interrupt flag bits (i.e., not using IRQ) or by being interrupted by IRQ. When an interrupt enable bit is a 1, IRQ is asserted and the appropriate interrupt active bit set to a 1 when the corresponding interrupt condition occurs.

The basic sources for IRQ generation are status change detected (status bit changes state, maskable in DSP RAM), configuration change implemented, receive buffer full, transmit buffer empty, and memory access (also maskable in DSP RAM). Each source is individually maskable. Table 4-6 identifies the interrupt sources and describes the interrupt clearing procedures.

4.5.2 Auto Dial Procedure

The host auto dial procedure is the same as outputting data to be transmitted using TBUFFER (Figure 3-2). The modem timing accounts for the DTMF tone duration and amplitude, and inter-digit delay. These dialing parameters are host programmable in DSP RAM.

Calling tone on/off times are also programmable in DSP RAM. Calling tone levels are controlled by the Transmit Level bits (TLVL).

The levels of the high band and low band DTMF tones may be modified by the host in DSP RAM. The level of the high band DTMF tone should be 2 dB greater than the level of the low band DTMF tone. Transmit Level bits do not affect DTMF levels.

The auto dialer default parameters are given in

Table 4-7.

Table 4-6. Interrupt Request Bits

Interrupt Active Bit	Interrupt Enable Bit	Interrupt Flag Bit	Interrupt Condition Description	Interrupt Clear Procedure
NSIA	NSIE	NEWS	New status detected (NEWS transitioned from a 0 to 1) a. RAM read or RAM write occurred b. Status bit changed in register 0A-0F, 01, 12, 14, 16-17, 1A, or 1B	Host writes a 0 into NEWS (Clears NSIA to a 0)
NCIA	NCIE	NEWC	New configuration implemented by the modem (NEWC transitioned from a 1 to a 0).	Host writes a 0 into NCIE (Clears NCIA to a 0)
TDBIA	TDBIE	TDBE	TBUFFER is empty and can be written (TDBE transitioned from a 1 to a 0)	Host writes to BUFFER (register 10:0-7) (Clears TDBE and TDBIA to 0)
RDBIA	RDBIE	RDBF	RBUFFER is full and can be read (RDBF transitioned from a 0 to a 1).	Host reads RBUFFER (register 00:0-7) Clears RDBF and RDBIA to 0)

Table 4-7. Auto Dial Default Values

Parameter	Default Value
DTMF Tone Duration	92 ms
DTMF Interdigit Delay	72 ms
DTMF Total Output Power Level	0 dBm
DTMF Low Band Power Level	–4 dBm
DTMF High Band Power Level	–2 dBm
Pulse Relay Make Time	36 ms
Pulse Relay Break Time	64 ms
Pulse Interdigit Delay	750 ms
Calling Tone On Time	500 ms
Calling Tone Off Time	2 s

DIal Digits/Tone Pairs

Hex	Dial Digit	Tone Pairs	
		Tone 1	Tone 2
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	#	941	1477
0C	A	697	1633
0D	B	770	1633
0E	C	852	1633
0F	D	941	1633
10	1300 Hz Calling Tone		
11	1100 Hz Calling Tone		

NOTE: Calling tone is continuously transmitted with the appropriate on-off time until NEWC is set or FFh is written into TBUFFER.

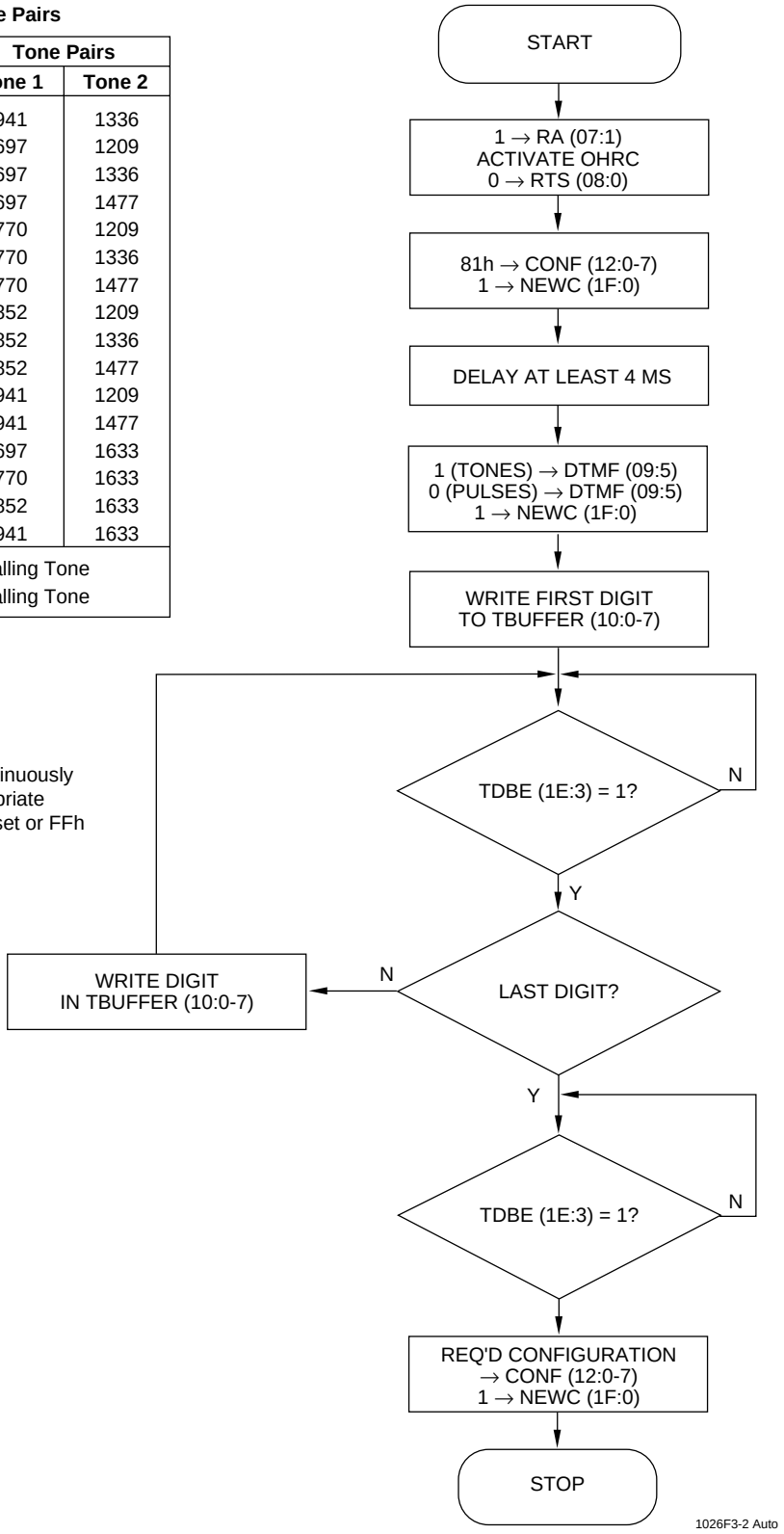

Figure 4-7. Auto Dial Sequence and Dial Digits

4.6 Eye Quality Monitor (EQM) and Automatic Rate Adaptation (ARA)

Eye Quality Monitoring (EQM) is often a good measurement of the line condition and typically has significant influence on the appropriate data rate and expected error rate. This section provides an overall view (see Figure 4-8) of the capabilities and parameters that can be controlled by the host.

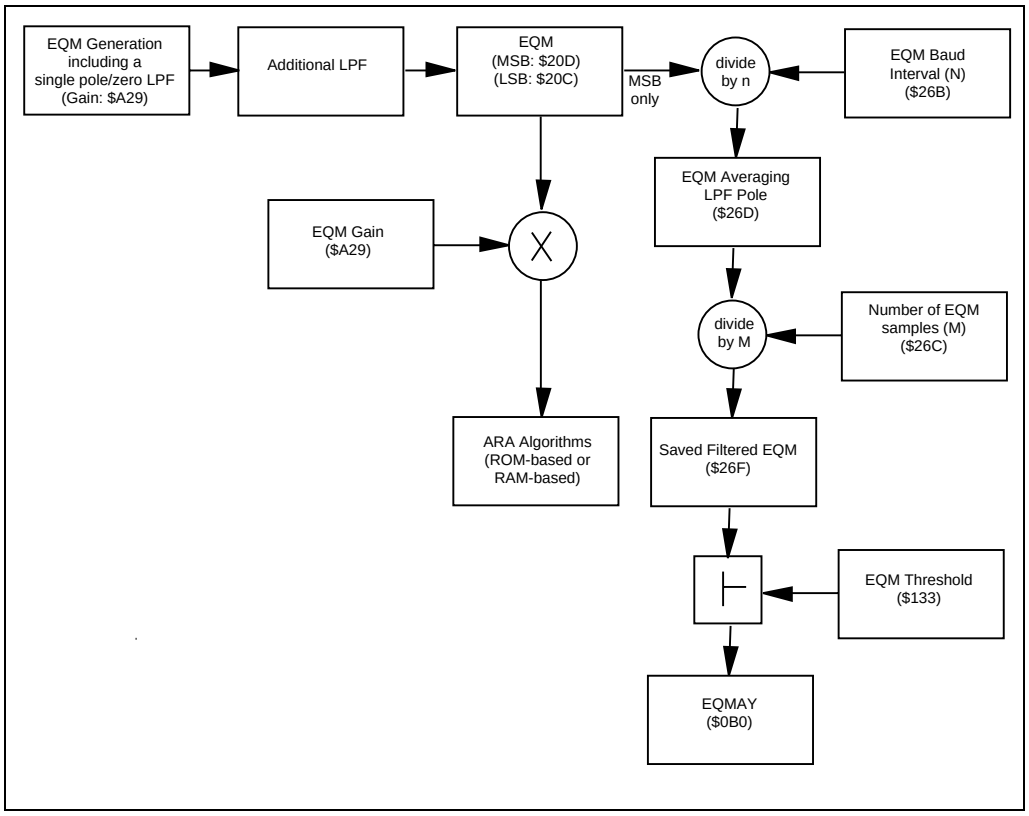

Figure 4-8. Block Diagram of EQM, EQM Averaging, EQM Above Threshold, and ARA Input

4.6.1 EQM

In V.29 and V.27 modes, EQM is the filtered squared magnitude of the error vector. For V.34, V.17, and V.33 modes (i.e.,, TCM modes), EQM is the filtered minimum trellis path length (or metric) which gives a better indication of signal quality for trellis modes.

The error vector formed by the decision logic can be used to indicate relative signal quality. As signal quality deteriorates, the average error vector increases in magnitude. By calculating the magnitude of the error vector and filter the results, a number inversely proportional to signal quality is derived. This number is called the eye quality monitor (EQM). Because of the filter time constant, EQM should be allowed to stabilize for approximately 700 baud times following RLSD going active or read near the end of V.34 training (TRN).

The EQM value for the non-trellis configurations is the filtered squared magnitude of the error vector and represents the average signal power contained in the error component. The power is directly proportional to the probability of errors occurring in the received data and can be used to implement a discrete Data Signal Quality Detector circuit (circuit 110 of CCITT Recommendation V.24 or circuit CG of the RS-232-C standard) by comparing the EQM value against experimentally determined criteria (Bit Error Rate curves). Figure 4-9 illustrates the relationship of the EQM number to an eye pattern created by a 4-point signal structure (e.g., V.29/4800 bps) in the presence of high level white noise. The EQM value is proportional to the square of the radius of the disk around any ideal point. The radius increases when signal to noise ratio (SNR) decreases. As the radius approaches the ideal point's boundary values, the bit error rate (BER) increases. Curves of BER as a function of the SNR are used to establish a criteria for determining the acceptability of EQM values. Therefore, from an EQM value, the host processor can determine an approximate BER value. If the BER is found to be unacceptable, the host may cause the modem to fallback to a lower speed to improve BER.

It should be noted that the meaning of EQM varies with the type of line disturbance present on the line and with the various configurations. A given magnitude of EQM in V.29/9600 does not represent the same BER as in V.27/4800. The former configuration has 16 points that are more closely spaced than the four signal points in the latter, resulting in a greater probability of error for a given level of noise or jitter. Also, the type of line disturbance has a significant bearing on the EQM value. For example, white noise produces an evenly distributed smearing of the eye pattern with about equal magnitude and phase error while phase jitter produces phase error with little error in magnitude.

Since EQM is dependent upon the signal structure of the modulation being used and the type of line disturbance, EQM must therefore be determined empirically in each application.

A typical eye pattern generation circuit is shown in Figure 8-5.

Note that the eye pattern is not displayed when 2800 or 3429 baud is selected in V.34 modes. The use of precoding and shaping in V.34 modes will distort the eye pattern's appearance, even under ideal conditions. The EQM value should be monitored in V.34 modes to determine the quality of the connection.

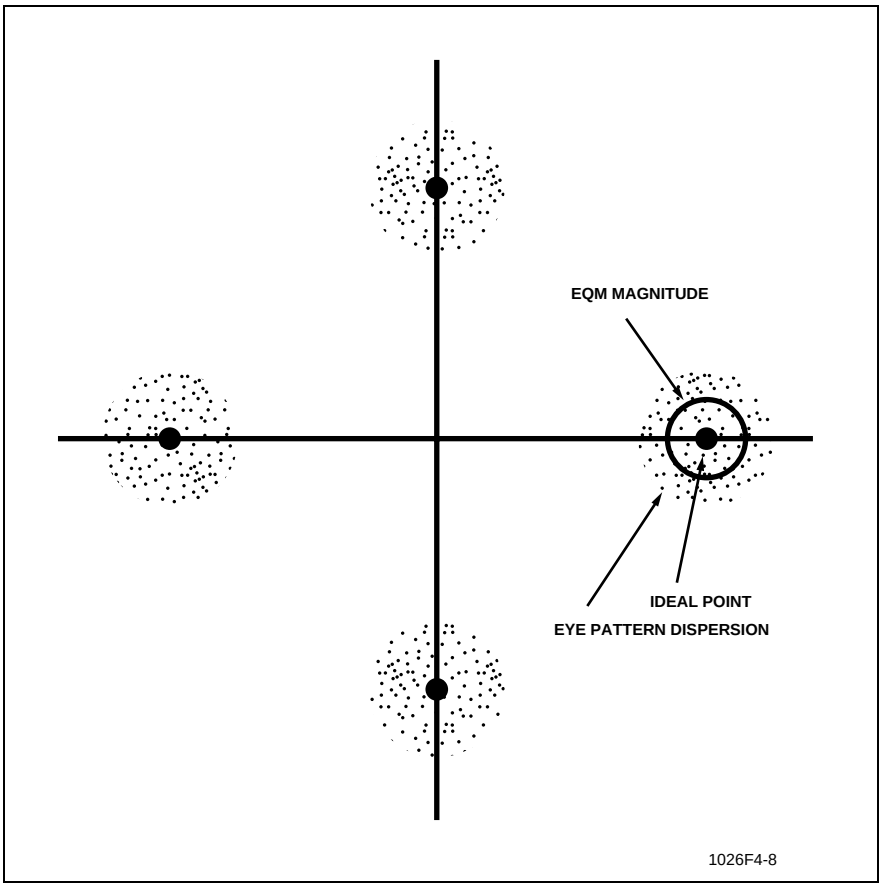

Figure 4-9. Relationship of EQM to Eye Pattern

4.6.2 Automatic Rate Adaptation

The automatic rate adaptation (ARA) algorithm selects the initial V.34 primary channel data rate based on the level of EQM. ARA is enabled by setting the EARC bit (15:0), which defaults off.

For the initial data rate selection, the EQM is checked towards the end of the training, just before the rate negotiation. The 4-point or 16-point EQM is compared against a table of values representing the necessary levels to achieve the corresponding data rates with an EQM of around 2000h. Once the maximum achievable rate is determined, the CONF register is changed to reflect the estimate, and is then used to suggest a data rate in the following negotiations.

In general, there are two methods the host may choose to modify how EQM values are used with ARA. The first method is to modify the EQM value that is presented to the ARA algorithm by modifying the EQM gain, and the second method is to modify the ARA thresholds (so called ARAinRAM).

Modifying the EQM Gain

The second method to affect these rate adjustments is to increase the EQM gain at address A29 for a more reliable connection or to lower the EQM gain for a less reliable connection. The default value is 1000h. This method affects the EQM reading at address 20C. In V.34, the EQM gain may be changed after the SDET bit is set.

Example 1: If a more reliable (lower speed) connection is desired, increase the EQM gain from the normal value of 1000h to 2000h. The rate selected would then be one lower, e.g., 21600 will be selected whereas 24000 would have been selected without the change.

Example 2: If a less reliable (higher speed) connection is desired, decrease the EQM gain from 1000h to 0800h. Modification of the ARA thresholds is described in paragraph 4.6.5.

4.6.3 EQM Averaging

A host-programmable EQM averaging feature helps the host controller to initiate data rate change decisions. A single pole low pass filter is used to average the MSB of EQM samples. The number of symbol intervals between EQM samples is host-programmable in memory location $26B (EQMBaudInterval). The pole position is located at RAM $26D and can take a range of 0- 7F. Also, the host can program the number of EQM samples to run through this filter before the final filtered EQM value (FilteredEQM) is determined. The EQMAT bit is set if this final FilteredEQM ($26F) is larger than the EQMAT threshold (RAM $133). If EQMBaudInterval is 0, then the EQM averaging is disabled as is by default. Suitable values for addresses 26B, 26C and 26D are 20h, 64h and 60h, respectively. They may be altered as desired. All RAM accesses are 8 bit.

Name	Address	Default	Description
EQM Baud Interval	26B	0	Symbols between EQM samples used as input to LPF
Num EQM Samples	26C	0	EQM samples to be run through the EQM LPF
EQM Pole	26D	0	Determines the bandwidth of the EQM low pass filter
Saved Filtered EQM	26F	-	Output of EQM filter used for EQMAT determination (MSB value)

4.6.4 Default V.34 ARA threshold (ARA in ROM)

When not using ARAinRAM, the highest data rate for each symbol rate is:

Symbol	Highest Data Rate (kbps)	Possible rate in revised V.34 (kbps)
3429	33.6	33.6
3200	28.8	31.2
3000	26.4	28.8
2800	24.0	26.4
2400	21.6	21.6

(The host may wish to use ARAinRAM to negotiate the higher data rates for the 3200, 3000, and 2800 symbol rates.)

4.6.5 Programmable ARA Thresholds (ARA in RAM)

A host selectable and configurable method for changing the EQM thresholds for the Automatic Rate Adjust (ARA) is available in the data pump. This feature applies to V.34 mode only. The 'ARAinRAM' function is enabled by setting bit 4 of RAM address 3A5. (8-bit access). Sixteen RAM locations have been allocated for the ARAinRAM thresholds. These occupy locations 3B0 to 3BF.

The search table used for determining the best data rate for a given EQM has been organized uniquely. The search through the table starts at the low address first, which represents the lowest data rate1, and progresses through to the higher data rates as the measured EQM value during training decreases. The final measured EQM is compared to the ARA RAM table. The EQM value must be greater than the threshold value in RAM for the corresponding data rate to be selected. For example, in the table below, if the final measured EQM were between 0088 and 00E0, the data rate of 26.4k would be selected. If the EQM value were less than 0088, the data rate of 28.8k would be selected. As another example, to allow more aggressive 28.8k connections, the threshold under the 26.4k rate (0088) should be increased. This would require the measured EQM to be slightly worse before falling back to 26.4k.

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[1] Normally for symbol rates above 2400 baud, the starting point is at 3B1hex and the initial data rate is 4800 bps. For the case of 2400 baud, the starting point is at 3B0h and the initial data rate is 2400 bps.

At the low data rates only the most significant byte of EQM is used in the threshold testing. However, as the thresholds get smaller for the higher data rates, it is necessary to use the least significant byte of EQM for the required resolution. When this transition occurs the table of thresholds must contain a 0, followed by the appropriate low byte threshold value. The last location to be searched must contain a 0 to stop further searches.

The following table of default thresholds against data rates is used in the ARAinRam function. Note that by default, the 31.2k and 33.6k data rates are not included in the ARA selection process. The host must enter suitable values if those data rates are to be included in the selection process.

Data Rate (Kbps)	2.4	4.8	7.2	9.6	12.0	14.4	16.8	19.2	21.6	24.0	26.4	28.8	31.2	33.6
Threshold (hex)	2000	1A00	1200	0C00	0A00	0900	0500	0300	0200	0090	0028	0010	0004	0001

Consequently, the default values written into RAM are:

Address	Value	Comment
3B0	20	
3B1	1A	
3B2	12	
3B3	0C	
3B4	0A	
3B5	09	
3B6	05	
3B7	03	
3B8	02	
3B9	00	This 0 causes the search algorithm to use low byte of EQM.
3BA	90	The next threshold (it is equal to 00E0h).
3BB	28	
3BC	10	
3BD	04	
3BE	01	
3BF	00	The last valid entry in the table must be a 0.

Configuring the ARAinRAM Thresholds During the V.34 Handshake

The thresholds are designed for optimum connectivity at symbol rates of 3429 and 3200. Whereas this will cover the vast majority of connections, the user may wish to alter the ARAinRAM values when symbol rates of 3000 and below are required. In this situation a host can read the symbol rate and then load up a new set of ARAinRAM values into the address range specified. This is done at the start of Phase 3 of the handshake.

Method:

1. Monitor the Receive Handshake Status (Register 16, SECRXB). Wait until it is set to 4X.
2. Read the selected connection symbol rate (location 2E3, Function 60).
3. Write in appropriate ARAinRAM thresholds for that symbol rate in locations 3B0 through to 3BF, using the information provided above. (8-bit access)

Forced 2400 Symbol Rate when Probing SNR is Adverse

If the signal to noise ratio (SNR) is less than the specified threshold, the data pump overrides the bandwidth evaluation algorithm and forces the Symbol Rate to 2400 baud. This allows the modem to fall back to 2400 bps if the SNR is poor as defined by this threshold. The threshold is located in RAM at address 3C0 hex and the bit which enables this feature is at bit 5 of address 3A5 hex. The default for this bit is enabled and the default threshold value is 0Dh which approximates to a SNR of 12 dB. All RAM accesses are 8 bit.

4.7 Data Rate Selection

For V.34 half duplex modes, the data rate selection process is applicable in two situations: The initial primary channel data rate selected during the training process and primary channel data rate changes negotiated through the MPh exchanges (during control channel resynchronization) between pages. A block diagram of the data rate negotiation mechanism between the source and the recipient modem is shown in Figure 4-10. Each of the components will be discuss in this section.

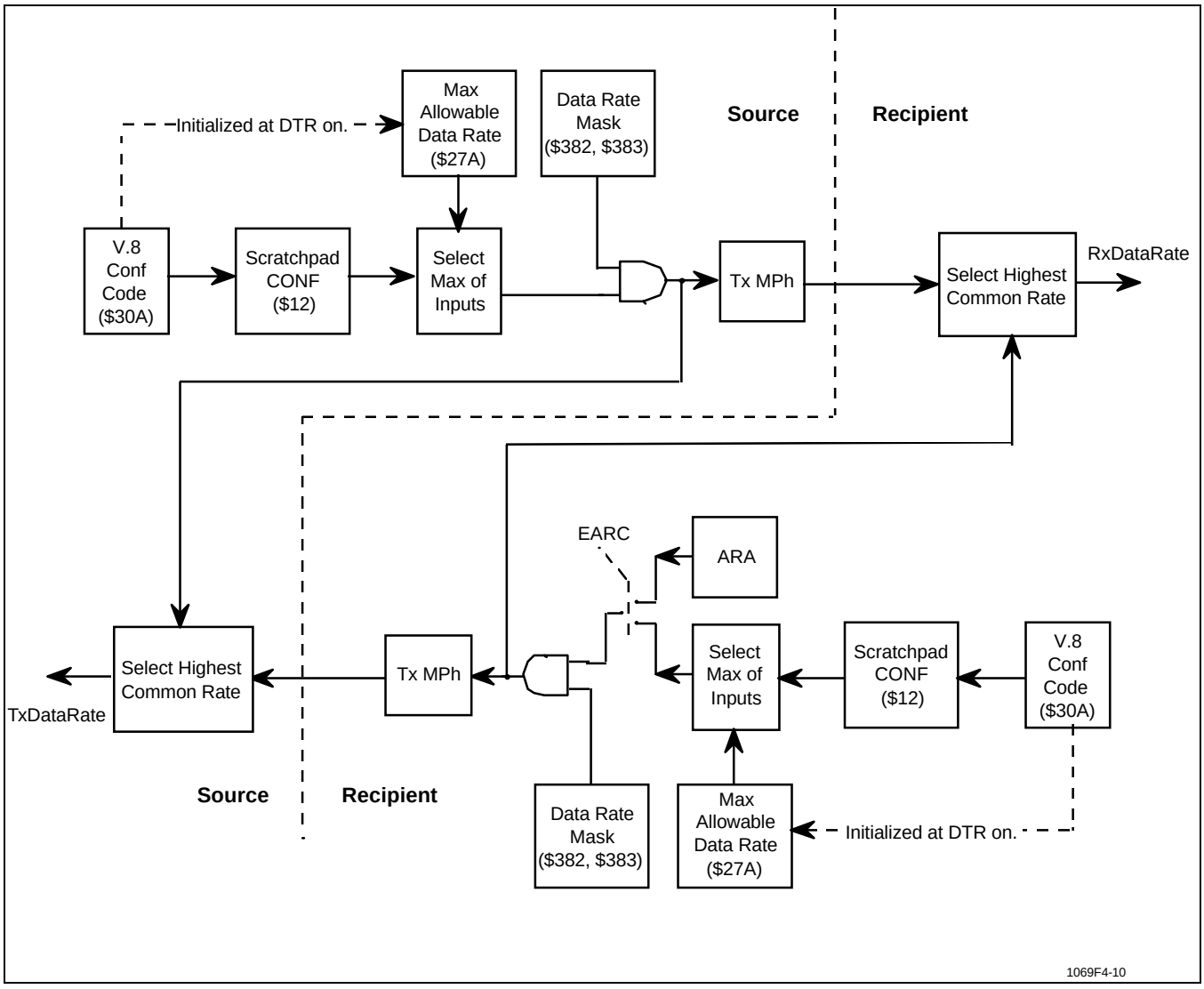


Figure 4-10. Data Rate Negotiation Mechanism

Several factors affect the final primary channel data rate selection upon initial training:

- The Data Rate Mask ($382, $383) in the source and recipient modem (Template for MPh bits 35 though 49)
- The setting of the EARC/ARC bits in the recipient modem only
- The post-V.8 preferred connection rate set in address $30A in both the source and recipient modems. (the setting of MPh bits 20:23 after considering the EARC/ARC bits)
- The maximum allowed data rate set in address $37A. Values for $37A are the same as the lower 4 bits of CONF for V.34 modes. The value in $37A defaults to $C (28.8k) and is automatically updated by the modem when DTR is set when CONF $AA (V.8).

In all cases, the highest common data rate of the following criteria is used.

- Rates that are disabled in the Data Rate Mask will never be negotiated.
- In the source modem, the maximum preferred initial connect rate is determined from $30A
- If EARC is not set in the recipient modem, the maximum preferred connect rate is determined from $30A.
- If EARC is set in the recipient modem, the maximum preferred connect rate is determined from the ARA algorithm.

For the primary channel data rate changes between pages, the initiating host should set the new desired rate in CONF and may need to adjust the value in $37A. The maximum preferred rate (MPh bits 20:23) is then determined from the CONF bits

of the initiating modem after taking account of the Data Rate Mask. The responding modem sets MPh bits 20:23 solely on the highest rate available in its data rate mask. EARC bits in either modem have no effect.

Data Rate Mask

The V.34 data rate masks occupy two bytes in RAM. Locations 382 and 383 represent the lower byte and the upper byte of the mask, respectively (Table 4-8). The bits in the mask represent the enabling of a particular data rate if set or disabled if reset. The definition of the bits are data rate 2400 is at bit 0 (i.e. the LSB of address 382), 4800 is at bit 1, 7200 at bit 2 and so on up to 33600 bps (in 2400 bps increments) which is bit 13 of the mask (or bit 5 of address 383). Bits 14 and 15 are reserved for future use (and must remain set to 1).

Table 4-8. V.34 Rate Sequence Mask Bit Assignments

Data Rate	V.34 Data Rate Mask-MSB (address 383)								V.34 Data Rate Mask-LSB (address 382)							
(bps)	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
2400	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	1
4800	-	-	X	X	X	X	X	X	X	X	X	X	X	X	1	X
7200	-	-	X	X	X	X	X	X	X	X	X	X	X	1	X	X
9600	-	-	X	X	X	X	X	X	X	X	X	X	1	X	X	X
12000	-	-	X	X	X	X	X	X	X	X	X	1	X	X	X	X
14400	-	-	X	X	X	X	X	X	X	X	1	X	X	X	X	X
16800	-	-	X	X	X	X	X	X	X	1	X	X	X	X	X	X
19200	-	-	X	X	X	X	X	X	1	X	X	X	X	X	X	X
21600	-	-	X	X	X	X	X	1	X	X	X	X	X	X	X	X
24000	-	-	X	X	X	X	1	X	X	X	X	X	X	X	X	X
26400	-	-	X	X	X	1	X	X	X	X	X	X	X	X	X	X
28800	-	-	X	X	1	X	X	X	X	X	X	X	X	X	X	X
31200	-	-	X	1	X	X	X	X	X	X	X	X	X	X	X	X
33600	-	-	1	X	X	X	X	X	X	X	X	X	X	X	X	X

4.8 Data Rate Negotiation Procedures

4.8.1 Introduction

The diagram below depicts the decision process of the V.34 half-duplex data rate negotiation. Firstly, a number of caution notes should be made.

- It is advisable that the source modem be configured to allow all available data rates and allow the receiver make the best and most informed decision. The receiver has access to all the probing and signal quality information which constitutes to help making the decision of the best data rate.
- Only the recipient modem is capable of performing any ARA decisions and only during the initial startup.
- It is highly advised that the host allow changes of data rate to be initiated by the recipient only. This will simplify the process and prevent conflicts between source and recipient.

4.8.2 Initial Data Rate Negotiation

Before Connecting the host must enter their preferred maximum data rate/configuration code into the V.8 CONF register. ($30A). This maximum data rate is transferred to the Maximum Allowable Data Rate Register ($37A) for later use in data rate negotiations. For the source modem it is advisable to set this to 28800 (or 33600 if allowed) and allow the recipient to make the decision of the final rate based upon the selected symbol rate, noise, channel characteristic etc.. Or to use ARA if it is enabled. After the V.8 negotiation, the CONF is loaded with the V.8 CONF Register. and this is used to determine the maximum data rate. All rates below this are assumed to be enabled unless the final selection is further modified by the Data Rate Masks. The modem then constructs the Mph and transmits it. At the Recipient the selection is also transmitted and the one it receives is compared, the modem then selects the highest common rate as the receiver data rate. At the Source, the same process is repeated to determine the transmitter data rate. If no common rate is found, the modem will return with the Abort code to initiate a GSTN Cleardown.

4.8.3 Between Page Data Rate Changes

During Primary channel (RTS on), if the recipient modem's CONF is changed, turning RTS off on the source modem will result in the handshake procedure described in Figure 26/V34 (ITU Recommendation v.34 document) and the data rate selected will be the highest common rate indicated by both modems.

The same procedure as described above is used by the source modem if it wishes to make a data rate change.

4.9 HANDSHAKE TIMEOUT TIMERS

If any part of the handshake is not detected, the modem will time out and abort the handshake. In this case, the transmitter will immediately stop sending the training sequence. Also, the modem, upon timing out, will load an error code into register 14 (ABCODE) of interface memory that indicates that point in the handshake the time-out occurred. The error code is not cleared even if the modem immediately goes into a new handshake after aborting. The user can observe this register during the handshake to determine if an abort occurred.

The user can progressively observe the handshake detector bits (AADET, ACDET, CCDET, etc.) to determine how the handshake is proceeding. The user can thus be interrupted at each step of the handshake progression.

The V.32 handshake error codes and their meanings are:

Error Code	Reason For Aborting (Time-out)
00	No error
01- FF	See ABCODE in 3.1.2 Interface Memory Signal Definitions, and Table 3-1 and Table 3-2. The individual bits in the interface memory are referred to using the format Z:Q. The register number is specified by Z (00 through 1F) and the bit number by Q (0 through 7, 0=lsb).

4.10 MODEM SELF-TEST INFORMATION

After a power-on reset, the modem performs a self-test of the internal controller and DSP devices. After each self-test, the test results and configuration information is loaded into interface memory.

Figure 4-11 shows the flowchart for reading the self-test data.

4.10.1 Controller Self-Test

The controller self-test is performed first. Upon test completion, the following test results and configuration information is loaded into interface memory:

Register	Function	Value (Hex)	Value Type
1D, 1C	RAM1 Checksum	EA3C	Constant
1B, 1A	RAM2 Checksum	5536	Constant
19, 18	ROM1 Checksum	5F4C	Constant
17, 16	ROM2 Checksum	3831	ASCII 48
15	Timer/ROM/RAM	08	Constant
13, 12	Part Number (Typ.)	3533 (for R6713-14) or 3534 (for R6713-20)	ASCII 53 or ASCII 54
11, 00	Revision Level (Typ.)	4241	ASCII BA

The host should read the test results within 5 ms of the appearance of RAM1 and RAM2 checksums. Register 10 should then be read to reset bit 1E:3 (ignore the read value).

When bit 1E:3 is reset or 5 ms has expired, the information is cleared and the DSP self-test is performed. If the register 10 is not read by the host, bit 1E:3 will not be reset.

4.10.2 DSP Self-Test

Upon completion of DSP self-test, the following test results and configuration information is loaded into interface memory and bit 1E:3 is set to a 1:

Register	Function	Value (Hex)	Value Type
1B, 1A	EC Checksum	02C0	Constant
19, 18	Multiplier Checksum	46EE	Constant
17, 16	RAM Checksum	B2A6	Constant
15, 14	ROM Checksum	3831	ASCII 68
13, 12	Part Number (Typ.)	3533 (for R6713-14) or 3534 (for R6713-20)	ASCII 53 or ASCII 54
11, 00	Revision Level (Typ.)	2041	ASCII A

The host should read the test results within 5 ms of bit 1E:3 being set.

When bit 1E:3 is reset or 5 ms has expired since DSP test completion, the information is cleared and modem initialization continues.

Soft Reset. If reading the self-test information by performing a soft reset (see SFRES in 3.1.2, Interface Memory Signal Definitions) and Table 3-1 and Table 3-2.

The individual bits in the interface memory are referred to using the format Z:Q. The register number is specified by Z (00 through 1F) and the bit number by Q (0 through 7, 0=lsb).set SFRES, then set NEWC (do not wait for NEWC to clear). Proceed as described above. After reading the desired information, wait for NEWC to clear before accessing the modem.

NOTE: The reset time for both a hard or soft reset is under 400 ms.

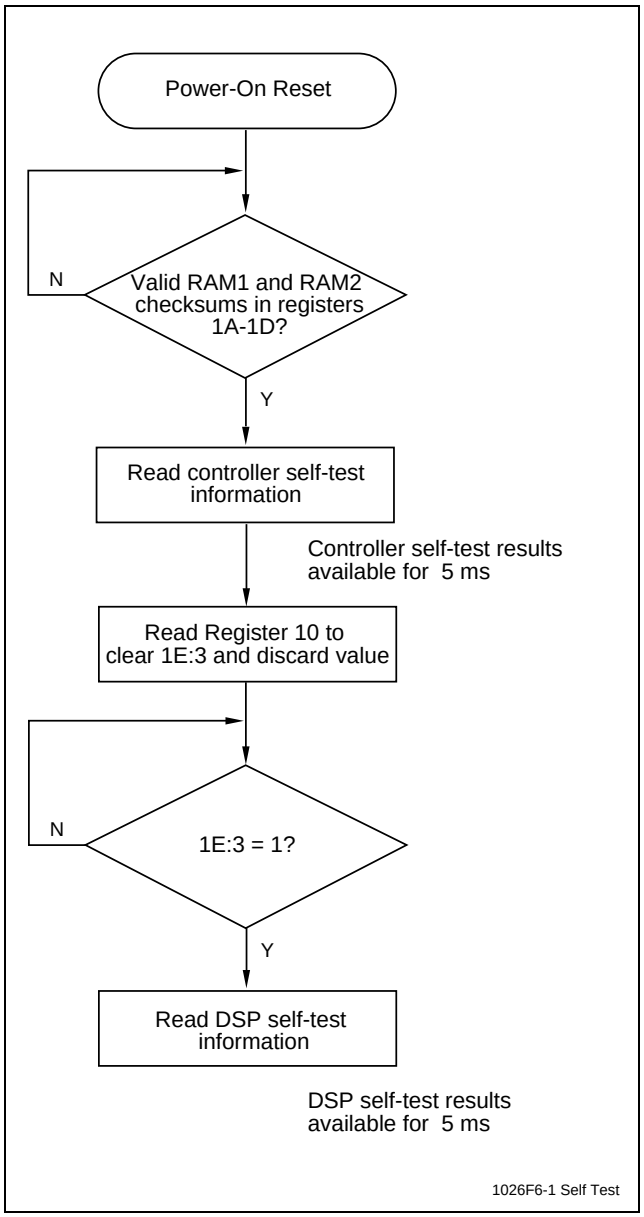


Figure 4-11. Modem Self-Test Results Read Procedure

4.11 Tone Detectors

A block diagram of the three tone detectors is shown in Figure 4-12. Tone detector C is preceded by a prefilter and a squarer. The purpose of the prefilter and squarer is to allow dual tones to be detected while rejecting the main channel energy. For example, TONEC can be programmed to detect a difference frequency generated by the squarer for detection of 350 Hz and 440 Hz. The prefilter would be designed to reject the energy in the 600 to 3000 Hz band. If the dual tone pair of 350 and 440 Hz appeared (or any other frequency pair in the range of 300 to 600 Hz with a difference of 90 Hz) TONEC would turn on.

The SQDIS bit (02:6) allows the squarer in front of tone detector C to be disabled. If the squarer is disabled then tone detector C will have four cascaded biquads (since there is a prefilter consisting of two biquads), forming an 8-order IIR filter with user programmable coefficients. To make the prefilter transparent (to use TONEC as a 4th order filter), write 7FFFh in coefficients A1 and write 0000 to all other biquad coefficients.

Figure 4-12 shows that the prefilter and the main filter sections of the tone detectors are fourth order (two second-order biquads in cascade), thereby allowing a wide variety of filter characteristics to be synthesized. The only limitation on these user-definable shapes is that their gain should be around unity at the pass frequencies to avoid problems of saturation at one extreme (gain too high) and digital noise at the other (gain too low). Computation of the filter coefficients can be performed by any infinite impulse response (IIR) filter design program which outputs the coefficients in cascaded second-order sections.

The default sample rate is 7200 Hz, however, in the V.8 or V.34 modes, the sample rate is changed to 9600 Hz and all filter coefficients are changed by the modem. A soft or hard reset is recommended after a V.34 connection to restore default filter coefficients.

The level detector in each of the tone detectors flags the detection of a tone if it is in the tone detector passband and if it is above an upper threshold defined by THRESHU. The tone detected flag will remain set until, or unless, the tone falls below a lower threshold defined by THRESHL.

The tone detectors are preceded by an AGC. The gain of the AGC may be read at address 8B9 (DUGAIN). By default, DUGAIN reaches its maximum gain, at a value of 7FFFh, when the receive level is -26 dBm or lower. Signal levels below -26 dBm are thus not affected by the AGC, therefore, the threshold comparator will see a decreasing signal level as the input signal is lowered. The THRESHU and THRESHL adjustments are limited to signal levels below the AGC cut-off point (-26 dBm). If the THRESHU value is adjusted to try to limit the detection threshold to -20 dBm, the AGC will not allow it.

To raise the AGC cut-off point, decrease the value in address BBB (DAGCRF). The DAGCRF default value is FF00h, which results in the -26 dBm cut-off. Decreasing DAGCRF to FE00 raises the AGC cut-off to -20 dBm, thus allowing THRESHU to be adjusted for a minimum detection level of -20 dBm or lower.

The AGC may be disabled by first writing 0 to address 9BB (DSRATE), then writing a 07FFh to address 8B9 (DUGAIN).

The first-order low pass filter in each level detector, defined by the coefficients LPGAIN and LPFBK, controls the response time of each tone detector. Normally, these coefficients will not require alteration, but if, for example, a rapid cadence must be detected on a tone, then the 3 dB cutoff is approximately the reciprocal of the on-time or off-time of the tone, whichever is shorter. Decreasing LPFBK will speed up the response time. If LPFBK is decremented, then LPGAIN should be increase by the same amount. The gain of the filter should be set to unity (LPGAIN + LPFBK + 7FFFh). The default response time is in the order of 0.01 seconds.

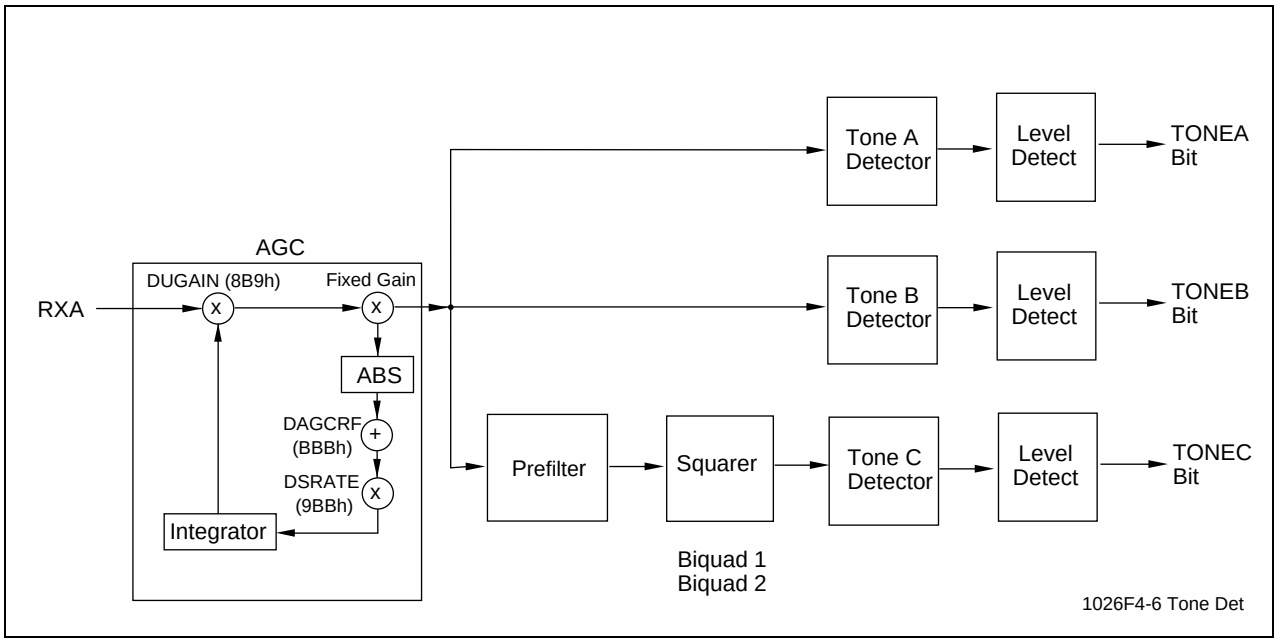


Figure 4-12. Tone Detectors

Example:

A call-progress tone detector is required for the US telephone network to detect appropriate tones that exceed –35 dBm.

Solution:

The requirement can be met by detecting tones in the 245 Hz-650 Hz range. A bandpass filter with a passband of 245 Hz-650 Hz must be designed. Any filter up to fourth order can be implemented and, normally, it is best to choose the highest order available, especially for bandpass designs. A biquad filter design package could carry out this function by defining the passband frequencies, the filter order, the filter gain (chose unity), and the filter sampling rate (7200 Hz). An example of suitable coefficients is:

Function	A1	A2	A3	B1	B2
Biquad 1	0.1368	–0.2736	0.1368	1.8281	–0.8835
Biquad 2	0.1368	0.2736	0.1368	1.5716	–0.7920

These values should first be divided by two because coefficients greater than one are unrealized in the actual filter implementation. This division should be done even if none of the coefficients in the design are greater than one. This is because the biquad sections have been implemented as shown in Figure 4-13. The modified values are, therefore:

Function	A1'	A2'	A3'	B1'	B2'
Biquad 1	0.0684	–0.1368	0.0684	0.9140	–0.4418
Biquad 2	0.0684	0.1368	0.0684	0.7858	–0.3960

Next, convert the above numbers to fractional 2s complement numbers. In this case, the default coefficient values for TONEA:

Function	A1'	A2'	A3'	B1'	B2'
Biquad 1	08C2	EE7C	08C2	74FE	C774
Biquad 2	08C2	1184	08C2	6495	CD4F

The second part of the requirement is to detect tones that exceed –35 dBm. The approximate values of THRESHU and the corresponding tone level detected for TONEA at 500 Hz are:

THRESHU (Hex)	Tone Level Detected (dBm)
1100	–29
0C00	–32
0880	–35
0600	–38

THRESHU should be 0880h. If no hysteresis is required in the tone detector, then set THRESHL to 0880 (see Table 4-3). If hysteresis is required, then make THRESHL < THRESHU. Threshold levels stated in the data sheets are measured at the band edges. Other filter designs may require different values to those shown above. Note that changing threshold coefficients may change the bandwidth response of tone detectors.

Table 4-9 shows the filter coefficient values for specific filters. Adjust THRESHL and THRESHU as necessary (see Table 4-3).

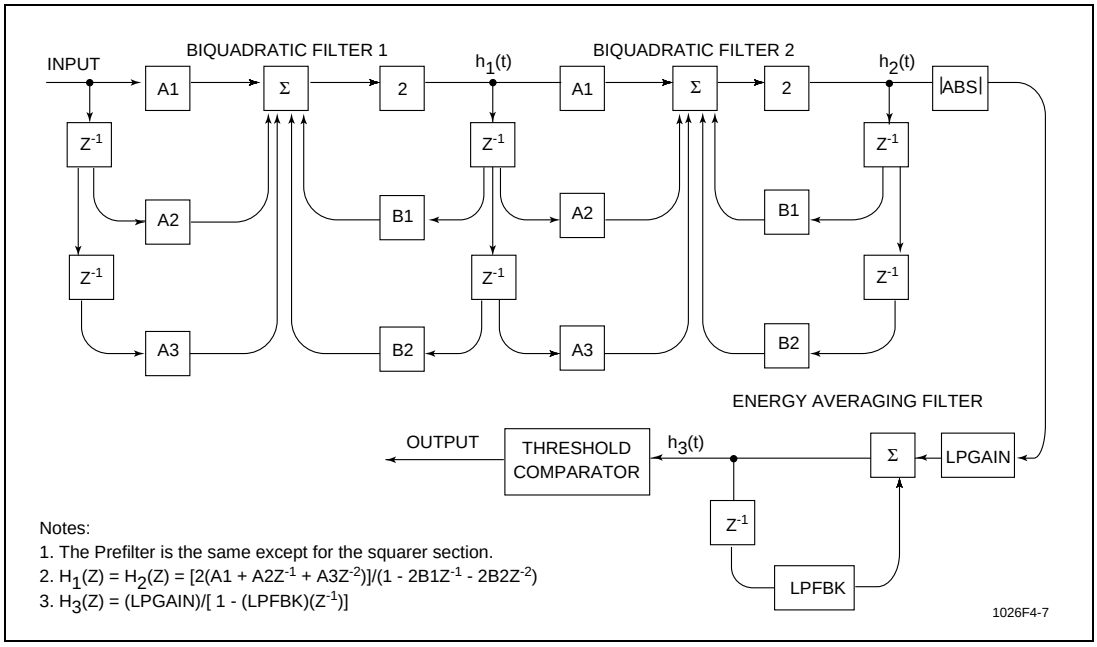


Figure 4-13. Biquad Filter and Level Detector

Table 4-9. Example Tone Detector Filter Coefficients

	Biquad1 Coefficients (Hex)					Biquad2 Coefficients (Hex)				
Sampling Rate/Filter	**A3**	**A2**	**A1**	**B2**	**B1**	**A3**	**A2**	**A1**	**B2**	**B1**
7200 Hz										
1100 Hz	01B3	FC9C	01B4	C147	48C6	01B3	0097	01B4	C147	4897
1800 Hz	0184	FCFB	0185	C147	001C	0184	01BD	0185	C147	FFE4
2250 Hz	0205	FBF9	0206	C147	CF9C	0205	0380	0206	C147	CF68
2100 Hz	01E8	FC32	01E9	C147	DF4F	01E8	034E	01E9	C147	DF19
2225 Hz	0205	FBF9	0206	C147	D22D	0205	0380	0206	C147	D1F8
1270 Hz	02B2	FAA1	02B3	C147	38A4	02B2	00F0	02B3	C147	3871
1650 Hz	0306	F9F9	0307	C147	10A6	0306	010D	0307	C147	106E
980 Hz	0205	FBF9	0206	C147	5337	0205	00B4	0206	C147	530D
1300 Hz	0244	FB7B	0245	C147	35A7	0244	00CA	0245	C147	3574
245-650 Hz[1]	08C2	EE7C	08C2	C774	74FE	08C2	1184	08C2	CD4F	6495
360-440 Hz[2]	0000	FD36	02CA	C63E	7243	02CA	0593	02CA	C63E	7243
9600 Hz (V.8 and V.34 Modes)										
1800 Hz	0372	FEA6	0372	C063	30D6	00C4	FFDA	00C4	C063	30D6
2250 Hz	0119	FE72	0130	C063	0C82	02D9	FEE3	02D9	C063	0C82
2100 Hz	0397	F8D3	0399	C3C9	1905	0397	02C0	0399	C3C9	176D
2225 Hz	0884	EF47	0889	C147	0E90	0884	FE54	0889	C147	0E66
1270 Hz	0123	FDBA	0123	C147	55B6	0123	00DF	0123	C147	5596
1650 Hz	028B	FAEA	028C	C289	3BDA	028B	01F3	028C	C289	3A68
980 Hz	0224	FBB8	0225	C289	64FF	0224	01A4	0225	C289	6403
1300 Hz	0112	FDDB	0113	C147	536D	0112	00D2	0113	C147	533D
245-650 Hz	F8EA	0000	0716	C63E	6FE1	0716	F5FB	0716	C774	7601
360-440 Hz	01AA	FEBC	01AA	C7CD	7438	FF5C	0000	00A4	C148	7A66

Notes:
1. TONEA default.
2. TONEB default.

4.12 Compromise Equalizer

The transmitter compromise equalizer can be programmed by the host in modes other than V.34 or FSK. The equalizer is a 30 -tap finite impulse response (FIR) digital filter. The first tap is at address $AED and the last tap is at $AD0. The sampling rate for the filter is 7200 Hz. New coefficients should be loaded while the modem is in the idle mode before turning on RTS. The coefficients have to be loaded only once. They are re-initialized to the default values only upon POR. The user should ensure that the overall gain of any filter designed is 1. Set NEWC bit after new taps have been loaded.

The configuration of the transmit CEQ is the standard canonic tap delay, coefficient and accumulator structure. Coefficients can be calculated with any number of techniques. If a Template design is required then a Remez Exchange Design can be used. or if one has the inverse Amplitude- Frequency Response then the technique of IFFT and Windowing can be used. In either cases the coefficients are not too difficult to determine. Care should be given to the scaling of the filter. The safest course is to ensure that the designed filter has unity gain.

Format: 16-bit, signed, 2s complement

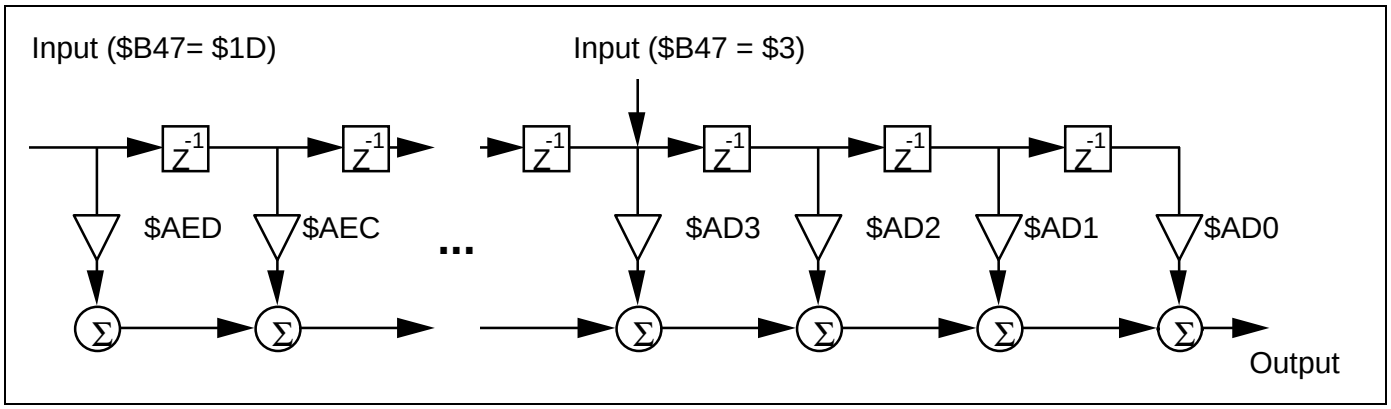


Figure 4-14. Compromise Equalizer

Table 4-10. Compromise Equalizer Taps

	JPN-4		No filter	
	Number of Taps (Addr=$B47)			
	$1D		$03	
Address (hex)	Value (hex)	Value (decimal)	Value (hex)	Value (decimal)
AED	$0714	0.05530	X	X
AEC	$0A10	0.07861	X	X
AEB	$121B	0.14145	X	X
AEA	$13B9	0.15408	X	X
AE9	$18B8	0.19312	X	X
AE8	$16BD	0.17764	X	X
AE7	$12E7	0.14767	X	X
AE6	$0E18	0.11011	X	X
AE5	$0050	0.00244	X	X
AE4	$FF80	-0.00391	X	X
AE3	$F0F1	-0.11765	X	X
AE2	$F757	-0.06766	X	X
AE1	$F84C	-0.06018	X	X
AE0	$FBBD	-0.03329	X	X
ADF	$12C0	0.14648	X	X
ADE	$FEF3	-0.00821	X	X
ADD	$19E0	0.20215	X	X
ADC	$F6C6	-0.07208	X	X
ADB	$F6F7	-0.07059	X	X
ADA	$F9CE	-0.04840	X	X
AD9	$DBEF	-0.28177	X	X
AD8	$22DC	0.27234	X	X
AD7	$F9F3	-0.04727	X	X
AD6	$19D5	0.20181	X	X
AD5	$1358	0.15112	X	X
AD4	$C001	-0.49997	X	X
AD3	$0324	0.02454	$4000	0.50000
AD2	$25BB	0.29477	0	0.00000
AD1	$FD6A	-0.02020	0	0.00000
AD0	$EC5A	-0.15350	0	0.00000

4.13 Receive Level Extension in V.17/V.29/V.27 modes

The specified maximum input receive level in all high speed configurations is limited to -9 dBm.

This limit can be extended up to approximately 0 dBm in non-V.34 high speed modes, i.e. V.17, V.29, or V.27ter, with the procedures described below. To achieve the best result, the receive level extension procedure should be implemented only when the input level exceeds a certain threshold . This threshold level is set by the host and should be between -10 and -15 dBm.

The extending procedure can be divided into two independent parts:

1. Measure the receive level and make a decision whether the workaround is needed.

2. Change the gain and threshold levels to accomodate the higher receive levels.

Both procedures are described below.

4.13.1 Measurement of the Receive Level

In ITU-T Recommendation T.30, a high speed (except V.34) mode reception is preceded by a V.21 Channel 2 exchange. In the R288F, V.21 Channel 2 reception is not limited to a -9 dBm input level and can receive at levels up to 0 dBm. The receiver host should measure and estimate the input level, while receiving V.21 Channel 2 information. This is done during the preamble reception, which is transmitted for 1 sec in accordance with ITU-T Recommendation T.30. This may be accomplished using the following steps:

A. Monitor RLSD and SYNCD bits. When SYNCD bit is set after RLSD bit, the preamble is being received.

B. Delay about 800 ms to allow the AGC Gain Word to stabilize.

C. Read AGC Gain Word from location $A00 (RAM Access Method 4) to determine the receive level estimate.

The receiving level (RL) can be estimated using the AGC Gain Word (N) as follows:

Equation: RL = (N/682.7 - 54) dBm

Where: N - is the decimal value of the hex number read from RAM

Example: if the hex number read is $6900, then N=26880 and the receive level is

RL = (26880/682.7) - 54 = -14.6 dBm

Note: The hex number read from the modem is applicable for calculation only when input level doesn't exceed -6 dBm. Above -6 dBm, the hex number read from the modem will saturate at $7FFF, and higher receive levels cann't be calculated based on N. This is not a limitation for the procedure since the threshold should be less then -10 dBm.

D. The measured level can now be compared against the host's threshold and if it is above the threshold, then the next step may be implemented.

4.13.2 Changing the Gain and RLSD ON and OFF Thresholds

If this receive level measurement procedure indicates a receive level that necessitates the use of an extended receive range, the following procedures should be executed when switching from V.21 Ch2 configuration to the high speed mode.

A. Place appropriate high speed configuration code in CONF register.

B. Set bit 2 in RAM location $10D (Read-Modify-Write operation, Acc Method 1). This will prevent the thresholds values from being overwritten to their defaults.

C. Write new values for the RLSD Turn-On threshold(RAM Location $134, $135, Acc Method 2) and RLSD Turn-Off threshold (RAM location $136,137, Acc Method 2)

D. Set NEWC bit and wait until it is reset by modem.

E. Write a new gain value in location $B3C (Acc Method 3). It is important to write this value after the NEWC has been set and reset back, otherwise it will be overwritten by the modem with the default value.

F. When returning to V.21 Channel 2 mode, reset bit 2 of $10D to allow the modem to overwrite RLSD threshold values. It is to be done before the host sets NEWC bit to initiate the V.21 Channel 2 configuration.

G. On disconnecting from the line, either reset the modem or reset bit 2 in RAM location $10D to allow the RLSD thresholds to be reset to the default values for the next connection.

The receive level measurement may be executed only once, when the receiver receives DCS sequence and need not to be repeated every time when switching between the high speed modes and V.21 Channel 2.

Steps A, B, C, D, E have to be included in the high speed configuration procedure and repeated every time when modem is reconfigured to the high speed receiving. Step F must be included in the V.21 configuration procedure and repeated every time when modem is configured to the V.21 Channel 2 mode, and before NEWC bit is set.

Note: The values in Table 4-11 and Table 4-12 are recommended for L8153-2 code release. (They are subject to change in the next code release.)

Table 4-11. Recommended Gain value

Speed/Conf	Parameter	Location	Default	New Value
V.17, V.29, V.27 ter All configurations	Gain	$B3C	$61D4	$3700

Table 4-12. Recommended RLSD Threshold values

Parameter	Location	Speed/CONF	Default	New value
RLSD TURN-ON THRESHOLD	$134, $135	V.17/B1	$2023	$1300
RLSD TURN-OFF THRESHOLD	$136, $137	V.17/B1	$2646	$1950
RLSD TURN-ON THRESHOLD	$134, $135	V.17/B2	$2129	$1320
RLSD TURN-OFF THRESHOLD	$136, $137	V.17/B2	$25AC	$1850
RLSD TURN-ON THRESHOLD	$134, $135	V.17/B4	$20A1	$1300
RLSD TURN-OFF THRESHOLD	$136, $137	V.17/B4	$2607	$1900
RLSD TURN-ON THRESHOLD	$134, $135	V.17/B8	$2027	$1270
RLSD TURN-OFF THRESHOLD	$136, $137	V.17/B8	$26E9	$1900
RLSD TURN-ON THRESHOLD	$134, $135	V.29/14	$0423	$0143
RLSD TURN-OFF THRESHOLD	$136, $137	V.29/14	$01B0	$0075
RLSD TURN-ON THRESHOLD	$134, $135	V.29/12	$03F3	$0133
RLSD TURN-OFF THRESHOLD	$136, $137	V.29/12	$01C6	$0070
RLSD TURN-ON THRESHOLD	$134, $135	V.29/11	$038E	$0103
RLSD TURN-OFF THRESHOLD	$136, $137	V.29/11	$1CC	$0065
RLSD TURN-ON THRESHOLD	$134, $135	V.27ter/01	$1F48	$11F0
RLSD TURN-OFF THRESHOLD	$136, $137	V.27ter/01	$1EC9	$1169
RLSD TURN-ON THRESHOLD	$134, $135	V.27ter/02	$1F71	$1210
RLSD TURN-OFF THRESHOLD	$136, $137	V.27ter/02	$1FAF	$1250

5. HDLC OPERATION

The HDLC (High Level Data Link Control) protocol is a standard procedure used for data communications. SDLC (Synchronous Data Link Control) is a bit-oriented protocol which is a subset of HDLC. The same format is used in both protocols although all SDLC fields must be eight-bit octets. The modem uses the SDLC protocol but it is referred to as HDLC to avoid confusion. This protocol is used for both V.34 and non-V.34 data transmission. The binary coded procedural data are transmitted using the control channel (V.34 operations) or V.21Ch2 (non-V.34 operations).

5.1 HDLC FRAMES

Data and control information on a HDLC link are transmitted via frames. These frames organize the information into a format specified by an ISO standard that enables the transmitting and receiving stations to synchronize with each other. This format is shown in Figure 5-1. Flags and the frame check sequence are distinguished from the other fields by status bits in the modem interface memory.

Flags

All frames start and end with a flag sequence. The beginning flag and the ending flag are defined by the bit pattern 01111110 (7E). The ending flag for one frame can also serve as the beginning flag for the following frame. If separate ending and beginning flags are used, the final zero in the ending flag of one frame may also serve as the first zero of the beginning flag in the following frame. This process is known as "zero-sharing". The zero-sharing bit pattern is 011111101111110.

Address Field

The address field informs the receiver where the information is to go (if the primary station is transmitting) or where the message originated (if a secondary station is transmitting). This field is eight bits in length for the "basic" format.

For the "extended" format, the length is N number of octets, each octet having the first bit a binary zero with the exception of the last octet that begins with a binary one.

Control Field

The control field defines the function of the frame. It may contain a command or response. The control field might also contain send or/and receive sequence numbers. This field can be in one of the following formats:

1. Information Transfer Format
2. Supervisory Format
3. Unnumbered Format

This field is normally eight bits in length. Certain protocols allow for an extended control field of 16 bits in length.

Information Field

The modem does not distinguish between the address field, the control field, or the information field. The information field does not have a set length; however, this field is in the SDLC protocol format of 8-bit bytes.

Zero Insertion

Since flags mark the beginning and ending of a frame, some method must be implemented to inhibit or alter the transmission of data that appear as flags. The method used is called "zero insertion". HDLC procedures require that a zero be transmitted following any succession of five continuous ones. This includes all data in the address, control, information and Frame Check Sequence (FCS) fields. Use of zero insertion denies any pattern of 01111110 to ever be transmitted between beginning and ending flags.

The modem transmitter always performs zero insertion when in HDLC mode.

Zero Deletion

When transmitting flags, zero insertion is disabled. During reception of data, after testing for flag recognition, the receiver removes a zero that immediately follows five continuous ones. This is termed "zero deletion". A one that follows five continuous ones signifies either a frame abort (i.e., at least seven ones with no zero insertion) or a flag (i.e., 01111110). The sixth one is, therefore, not removed.

The modem receiver always performs zero deletion when in HDLC mode.

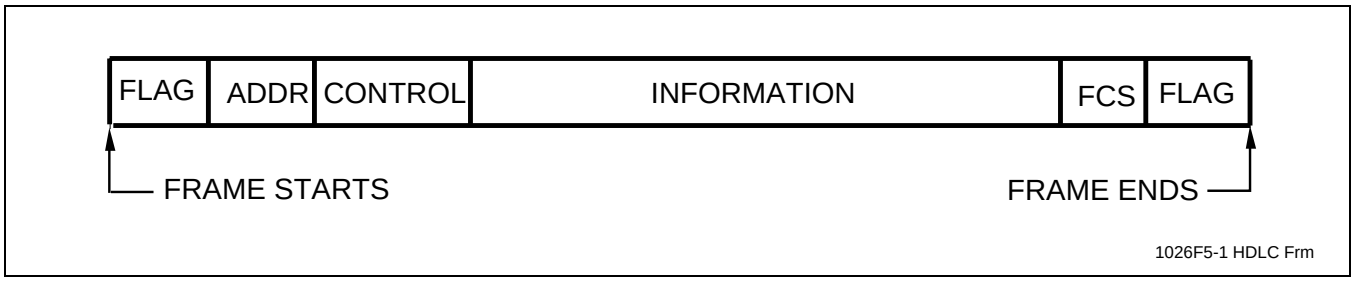


Figure 5-1. HDLC Frame

Frame Check Sequence

The purpose of the Frame Check Sequence (FCS) is to give a shorthand representation of the entire transmitted information field and to compare it to the identically generated shorthand representation of the received sequence. If any difference occurs, the received frame was in error and should be re-transmitted.

The FCS computation is done on all fields within the frame but does not include the flags. A standard Cyclic Redundancy Check (CRC) is used to compute the FCS. Either 16-bit (CRC16) (default) or 32-bit (CRC32) CRC may be selected using the ITU-T CRC32 RAM parameter (see parameter 52 in Section 4.4). The CRC polynomials are:

$$\text{CRC16} = x^{16} + x^{12} + x^5 + 1 \quad \text{(SDLC and X.25)}$$

$$\text{CRC32} = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + 1$$

The FCS is sent as two bytes of data immediately preceding the ending flag of the frame. The FCS register is first preset to all binary ones. The register is then modified by shifting in the data (no flags) contained in the address, control, and information fields. Following the last bit of data, the ones complement of the FCS register is transmitted as the FCS. The FCS is transmitted with the highest order bit first.

Frame Abortion, Frame Idle, and Time Fill

Frame abortion prematurely finishes transmission of a frame. This occurs by sending at least seven consecutive ones with no zero insertion. This abort pattern terminates a frame immediately and does not require a FCS or an ending flag.

An abort pattern followed by a minimum of eight additional consecutive ones idles the data link. Thus, seven to fourteen ones establish the abort pattern; fifteen or more ones constitute an idle pattern.

Interframe time fill is accomplished by transmitting continuous flags.

5.2 HDLC and FIFO Data Buffers

5.2.1 Transmit and Receive FIFO Data Buffers

Two 16-byte first-in first-out (FIFO) data buffers allow the DTE/host to rapidly output up to 16 bytes of transmit data and input up to 16 bytes of accumulated receive data. The receiver FIFO is always enabled. The transmitter FIFO is enabled by the FIFOEN control bit. The TXHF and RXHF bits indicate the corresponding FIFO buffer half full (4 or more bytes loaded) status. The TXFNF and RXFNE bits indicate the TX FIFO buffer not full and RX FIFO buffer not empty status, respectively. An interrupt mask register allows an interrupt request to be generated whenever the TXFNF, RXFNE, RXHF, or TXHF status bit changes state.

5.2.2 RX FIFO and HDLC Operation

The RXFIFO is a 12-bit wide FIFO; 8 bits for data and 3 bits of HDLC status (FE, PE, SYNCD). The bit OE is used to indicate an overrun condition and is set immediately upon an overrun condition, it is not buffered like the SYNCD, PE, and FE bits. If a byte is received as a FLAG, then 7E is stored in the data portion of the FIFO (RBUFFER) and the SYNCD bit is set (PE is set if there are CRC errors). (See Figure 5-2 and Figure 5-3.) The status bits must be read BEFORE reading the data bits because reading the data moves the FIFO pointer to the NEXT byte effectively overwriting the prior status bits.

If, in HDLC mode, 8 zeros appear at the receiver (intentional or otherwise), the HDLC processor will load them in the RX FIFO as data, but when the next flag is received a CRC error (PE set) will appear with it.

SYNCD will come on with the FIRST flag and the 7E will appear in the buffer. Again, when servicing the RDBF interrupt, the status bits (i.e., SYNCD must be read first.) The remaining 7Es, however long the string, will not be sent through the RX FIFO. The next data/error pair sent through the FIFO will be data (i.e., SYNCD off) or perhaps an abort (FE = 1).

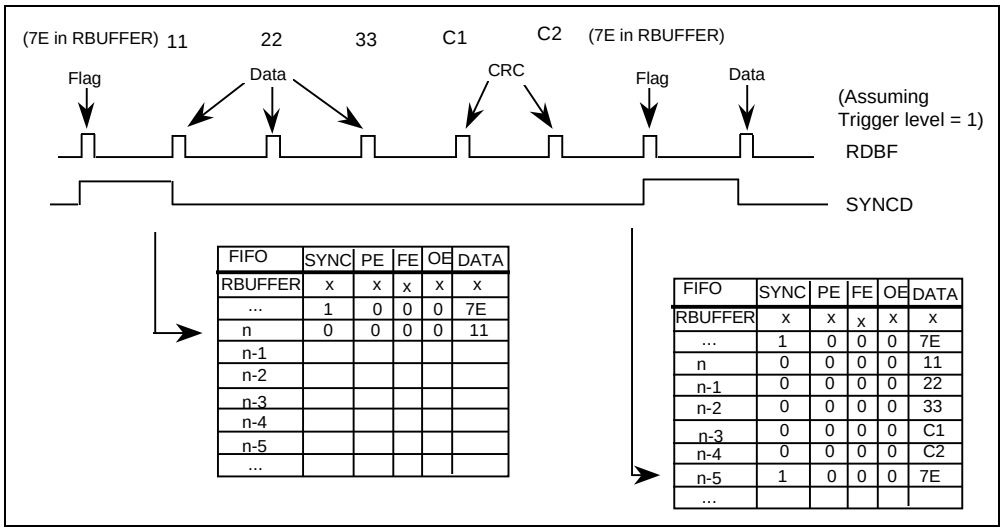


Figure 5-2. Normal HDLC Receive Operation

Note that the RDBF interrupts in the figures assume a trigger level of 1. If the trigger level is greater, the data bytes and status bits will still be loaded in the FIFO (at the same time as RDBF would have been set if the trigger level was set at 1) but RDBF will not be set.

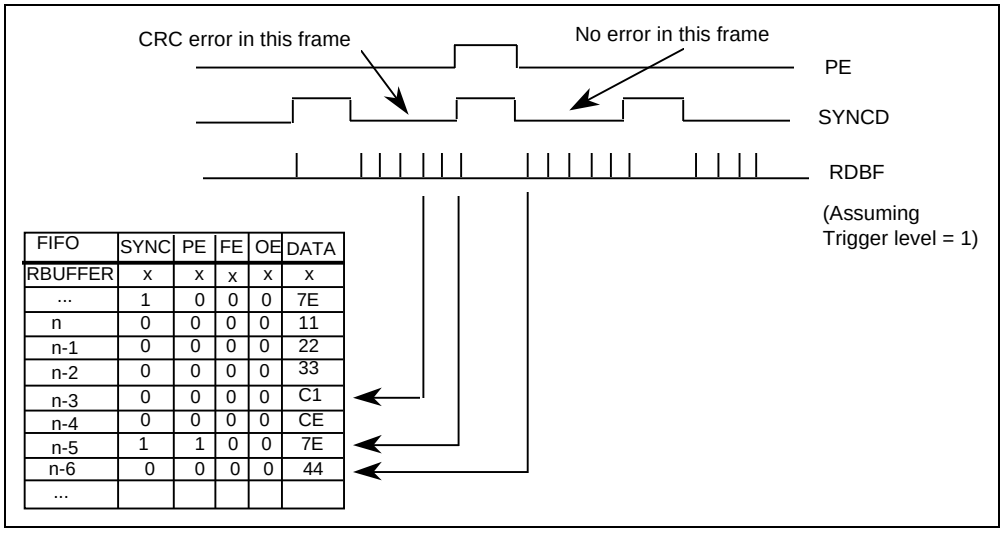
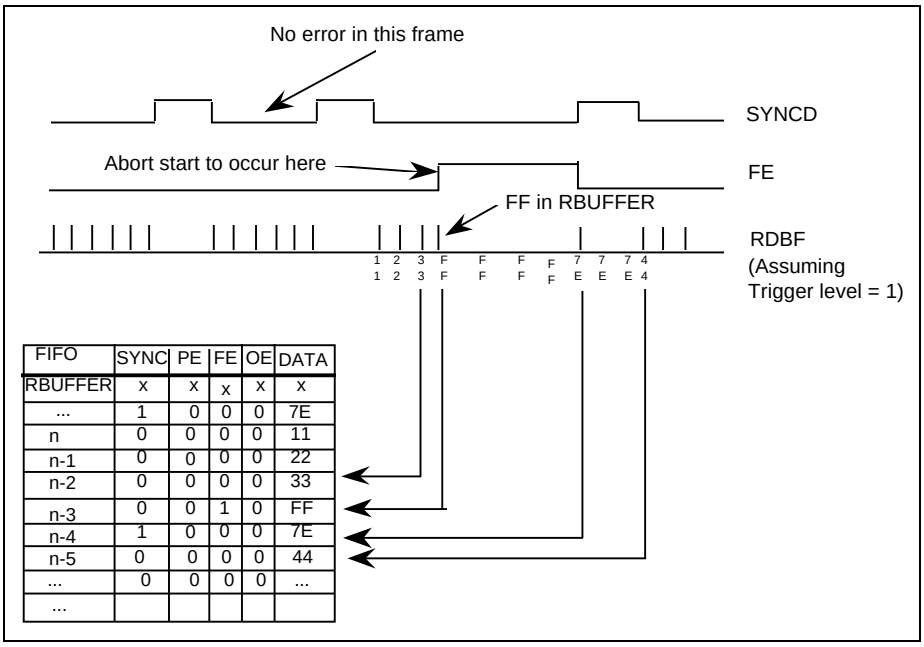


Figure 5-3. HDLC Receive Operation when a CRC error occurs.

The FE bit indicates that an abort has been detected. Figure 5-4 shows the relationship of the FE bit to the SYNCD bit. The modem will set only the FE bit when an abort is received. The modem will also provide an RDBF interrupt (assuming trigger level is 1) and the RBUFFER will contain a FFh which should be discarded. The FE bit will be cleared before receiving the first byte of the next valid frame.



FIFO	SYNC	PE	FE	OE	DATA
RBUFFER	x	x	x	x	x
...	1	0	0	0	7E
n	0	0	0	0	11
n-1	0	0	0	0	22
n-2	0	0	0	0	33
n-3	0	0	1	0	FF
n-4	1	0	0	0	7E
n-5	0	0	0	0	44
...	0	0	0	0	...
...					

Figure 5-4. HDLC receiver operation with an abort condition

The OE bit will be set when a received byte does not have room in the RXFIFO. That byte and all others that follow will not be placed in the RXFIFO as long as the RXFIFO is full. The OE bit must be reset by the host.

In many applications, there is little reason to enable NSIE when doing HDLC RX in this device. Simply use the RDBF (or RXHF or RXFNE). Read the status bits first. If SYNCD and FE are off, then read RBUFFER and store as data. When SYNCD is on, and PE is off, the last frame (if there was one) is valid. If SYNCD = 1 and PE = 1, then there were CRC error(s) in the last frame so trash it. If FE =1, then an abort condition has occurred so trash the frame.

Also make sure to purge the 7E from RBUFFER when SYNCD = 1 and also to purge the FFh when FE = 1.

5.3 OPERATION

5.3.1 Transmitter and Receiver Setup

To select HDLC mode, the host must:

1. Set the CONF bits to the desired modem configuration. HDLC can be used in all data modes except the full-duplex FSK modes (i.e., V.21 and V.23).
2. Set the TPDM bit to select Transmitter Parallel Data Mode (transmitting only). Setting TPDM is not required when receiving since received data is always available in RBUFFER. Note that HDLC transmission cannot be performed using the serial interface (TPDM = 0).
3. Set the RTS bit to turn on RTS (transmitting only).
4. Set the HDLC bit to select HDLC mode.
5. Set the NEWC bit.

5.3.2 Transmitter HDLC Operation

The format of the data input to the modem is in groups of 8-bit bytes. As in the normal synchronous parallel data mode, the least significant bit of the byte is transmitted first.

Flag Transmission and Reception

In HDLC mode, the modem will send continuous flags with no zero sharing (i.e., 0111111001111..) until the host loads data into the Transmit Data Buffer, TBUFFER (register 10). Thus, the modem defaults to transmitting time-fill and keeps the receiving link station active. The status bit FLAGS (0A:1) is set to indicate that the modem is transmitting the flag sequence.

In V.34 mode after executing the control channel start-up procedure defined in recommendation V.34 section 2.4, each station transmits HDLC flags using the control channel data rate determined during the control channel start-up procedure. At least two flags shall be sent prior to the first control channel frame after any starting resynchronization or retraining procedure.

Information Field Transmission and Reception

If the FIFO is not enabled (FIFOEN bit = 0), if the next byte is not loaded into TBUFFER within the next eight bit times, the modem interprets this as the end of a frame. If the FIFO is enabled (FIFOEN bit = 1), the TEOF bit must be set by the host to indicate that the next byte to be written into TBUFFER is the last byte in the frame. The host must reset the TEOF bit after writing the last byte of the current frame and before writing the first byte of the next frame.

FCS and Ending Flag Transmission and Reception

Following the detection end of frame, the modem automatically sends the FCS and ending flag. Status bit CRCS (0A:2)is set just before the highest order bit is sent to indicate that the FCS is being transmitted. Once the host sees this bit set, the first byte of the next frame can be loaded. In this case, the ending flag serves as the beginning flag for the next frame. The modem resets the CRCS bit when the ending flag is transmitted. At the same time, the modem sets the FLAGS bit.

After the FCS transmission (immediately following bit x0), the modem sends one flag to signify the end of the current frame and the beginning of the next frame. After the final zero in a flag is transmitted, the modem looks to see if the host has loaded new data into TBUFFER. If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag between frames is desired, the host must wait N-1 multiples of eight bit times after FLAGS is set by the modem to load new data into TBUFFER, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAGS is set by the modem.

Abort/Idle Sequence Transmission and Reception

An abort/idle sequence can be sent by the host setting the MHLD bit (07:0). The modem stops sending any normal frame transmission, as well as continuous flag transmission, and sends continuous ones. To stop sending continuous ones, the host must reset MHLD. Then, if no new data is loaded into TBUFFER, the modem sends continuous flags. If new data is loaded into TBUFFER, the modem sends a beginning flag and then the data in TBUFFER.

5.3.3 Receiver HDLC Operation

The format of the data output to the host is in groups of 8-bit bytes. As in the normal synchronous parallel data mode, the least significant bit of the byte is transmitted first.

Flag Transmission and Reception

The modem receiver continually searches for the flag data pattern. When one or more flags are detected, status bit SYNCD (0A:0) is set. The flags themselves are not presented to the host through the receiver data buffer RBUFFER (register 00). The host must service the RDBF interrupt while waiting for the SYNC bit to be set to a 1 in order to clear the Receive FIFO of any unwanted or left- over characters and to ensure the alignment of the SYNCD bit with the received flag.

The modem can also detect consecutive flags with zero-sharing.

Information Field Transmission and Reception

Received data between flags is passed to the host through the RBUFFER by the use of the handshaking bit RDBF (1E:0). The host must wait for RDBF to be set by the modem before reading the status bits, followed by the received data in RBUFFER. Note that the RBUFFER and Receive FIFO can accumulate 16 bytes before overflowing. If the host does not read the data within 16 byte times, the data in RBUFFER will be overwritten by the next received byte and the Overrun Error bit (0A:3) will be set. The flag sequence and abort/idle sequence are not presented to the user. The receiver determines where the FCS field is by detecting the ending flag. There is at least a 16-bit time delay in the reception of data.

FCS and Ending Flag Transmission and Reception

Upon the receipt of an ending flag in the current frame (which may also be the beginning flag of the next frame), the receiver checks the data in the FCS register. If the FCS register remainder is correct, the PE bit (0A:5) is left a zero. If the remainder is incorrect, the PE bit is set. The FCS field is also passed to the host, in case the host wishes to do his own CRC checking. The receiver will set the SYNCD bit and the PE bit (if the modem detected a frame with a bad CRC) after sending the FCS to the host. The modem presets the FCS register to all ones after one or more flags are received.

After the FCS transmission (immediately following bit x0), one flag is sent to signify the end of the current frame and the beginning of the next frame. After the final zero in a flag is transmitted, the modem looks to see if the host has loaded new data into TBUFFER. If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag between frames is desired, the host must wait N-1 multiples of eight bit times after FLAGS is set by the modem to load new data into TBUFFER, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAGS is set by the modem.

Abort/Idle Sequence Transmission and Reception

The modem receiver not only continually searches for flags, but also continually searches for an abort/idle sequence. When the modem detects this data pattern, it sets the FE bit (0A:4). The reception of data following the abort/idle sequence is treated as invalid data and is not presented to the host. Therefore, to re-establish transmitter and receiver synchronization, the receiver must see at least one flag. If FE is set, the current received data byte (typically FFh) should be discarded.

5.4 EXAMPLE OF NON-V.34 APPLICATION

Refer to Table 3-1 for a description of the bits associated with the HDLC functions. Figure 5-5 illustrates bit timing.

The bits in the interface memory are referred to using the format Z:Q. The register number is specified by Z (00 through 1F) and the bit number by Q (0 through 7, 0 = LSB).

5.4.1 Transmitter Example (Tx FIFO Disabled)

The steps to perform a typical HDLC transmission with the Transmitter FIFO disabled are (Figure 5-5a):

1. Set the modem configuration in CONF; reset the FIFOEN bit; set the HDLC, TPDM, and RTS bits.
2. The modem starts transmitting flags immediately and continues with flags until the first byte of data is loaded into TBUFFER.
3. Place the first byte of data into TBUFFER. The modem finishes transmitting the current flag followed by this byte of data.
4. As soon as TDBE is set, load in the next byte of data. This must occur within eight bit times of TDBE being set.
5. After all information but the last byte is given to the modem, load in the last byte of data in the frame as in step 4.
6. Wait until FLAGS is set to load in the first byte of the next frame. The modem follows the last byte of the current frame with the FCS and a flag.
7. Repeat steps 4 through 6 for all frames to be transmitted.

5.4.2 Transmitter Example (Tx FIFO Enabled)

The steps to perform a typical HDLC transmission with the Transmitter FIFO enabled are:

1. Set the modem configuration in CONF; set the FIFOEN, HDLC, TPDM, and RTS bits.
2. The modem starts transmitting flags immediately and continues with flags until the first byte of data is loaded into TBUFFER.
3. Place the first byte of data into TBUFFER. The modem finishes transmitting the current flag followed by this byte of data.
4. Continue to load data in TBUFFER until TXFNF = 0 or the last byte of the frame is reached.
5. After all information but the last byte is given to the modem, set TEOF, then load in the last byte of data in the frame as in step 4.
6. Reset TEOF to 0.
7. Repeat steps 4 through 6 for all frames to be transmitted.

5.4.3 Receiver Example

The steps to perform a typical HDLC reception are (Figure 5-5b):

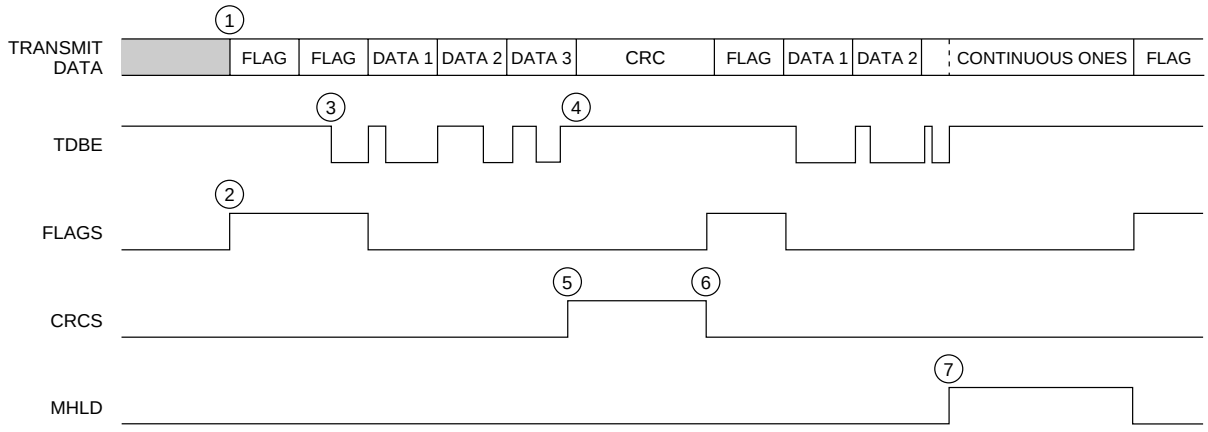
1. Set the modem configuration in CONF; set the HDLC bit. Then monitor, through interrupts, the RDBF, OE, SYNCD, PE, and FE status bits.
2. Wait for an interrupt. If it is caused by the modem setting RDBF (RDBIA is also set by the modem), if NEWS = 1 or NSIA = 1, read status bits OE, SYNCD, PE, and FE.

   OE indicates that RBUFFER was loaded with new data before the host read the old data.

   SYNCD indicates that the modem is receiving flags (RBUFFER = 7E).

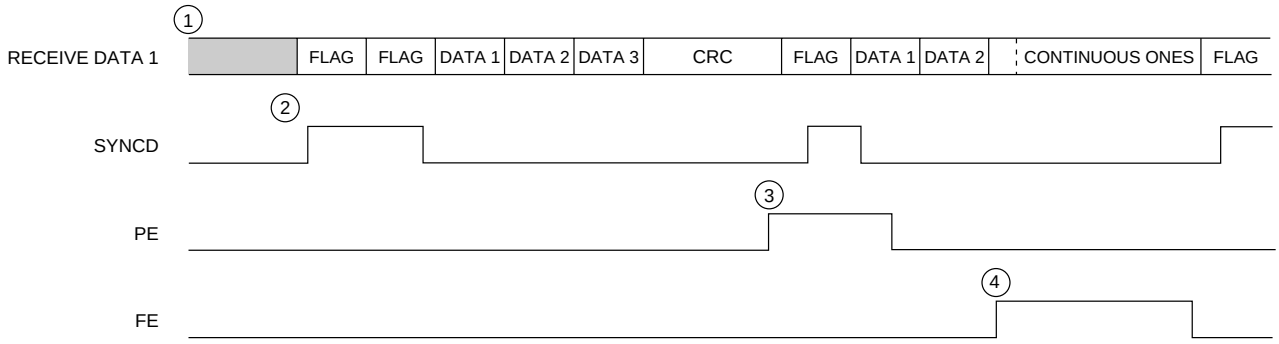
   PE indicates that the FCS had an incorrect CRC.

   FE indicates that an abort/idle sequence is detected (RBUFFER = FF) and the frame that was aborted is invalid. The modem does not set the PE bit in this case since no FCS checking is done.
3. If NEWS = 0 and RDBF = 1, read the received data in RBUFFER.
4. Continue waiting for interrupts and take appropriate action when the interrupts are received.



1. The host enters HDLC mode by setting HDLC bit.
2. The modem sets FLAGS prior to sending the first bit of the first 7E flag.
3. If the host loads the first data byte into TBUFFER while FLAGS is being sent, the data will not be sent until the flag is completely sent.
4. After TDBE is set, the host has 2.5 bit times to load new data into TBUFFER.
5. CRCS is set as soon as the last bit of the last data byte is sent and prior to sending the first bit of the CRC sequence. As soon as FLAGS is set, a new data byte of the next frame can be loaded.
6. CRCS is reset and FLAGS is set when the last bit of the CRC sequence is sent.
7. If MHLD is set anytime during the data, CRC, or flag transmission, the byte transmitted is interrupted and the abort sequence is started.

a. Transmitter (FIFOEN = 0)



1. Timing refers to when received data is presented to the host. Flags and the abort sequence are not presented to the host.
2. SYNCD will turn on 8-15 bit times after entering HDLC mode, when 7E flags are detected.
3. PE is set only if a bad CRC is detected by the modem.
4. FE will turn on when seven consecutive 1s are detected.

b. Receiver

1026F5-2 HDLC Timing

Figure 5-5. HDLC Signal Timing

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6. T.30 IMPLEMENTATION

6.1 General

ITU-T Recommendation T.30 details procedures for facsimile transmission over the PSTN. This standard describes how to initiate, complete, and end a fax transmission. This section describes methods to set up host software to implement T.30 with the modem.

A basic block diagram of a Group 3 facsimile machine is shown in Figure 6-1. The modem performs the modulation/demodulation process. The fax machine manufacturer must implement the interface between the modem (T.30), the data compression/decompression (T.4), and the interface to the scanner and printer.

There are five phases (A-E) to the T.30 facsimile protocol. Phase A is the call setup, in which both facsimile machines connect to the line. Phase B is a pre-message procedure which consists of identification and command sections. The actual high speed message transmission occurs during Phase C. This is followed by the post-message procedure or Phase D. Both facsimile machines release the line in Phase E.

This basic concept is true for both v.34 mode and traditional non-v.34 modes, such as v.17, v.29 and v.27 ter. There are differences in start-up procedures, turn-around polling procedure, etc. These differences are related to the fact that, in v.34 mode, start-up scenarios (Phase A) involve v.8 procedures, v.34 line probing and parameter exchange. The original v.21 start-up, after CNG-CED exchange, goes directly to handshake procedures (Phase B). This section describes T.30 procedures using v.21 Channel 2. The v.8 and v.34 procedures are described in Chapter 7.

6.2 V.21 Channel 2 Operation

Figure 6-2 illustrates a typical Group 3 facsimile procedure. This example on T.30 describes a facsimile call where the calling unit (originate) transmits a documents to a called unit (answer). Phase E is not included in this example since it is the call release and both ends hang up.

Figure 6-3 through Figure 6-7 illustrate how to originate a fax call. Figure 6-8 through Figure 6-13 illustrate how to answer a fax call. Figure 6-14 through Figure 6-19 illustrate subroutines for originating or answering a fax call.

6.2.1 Phase A

T.30 specifies that call establishment can be realized one of four ways. The four methods of call establishment are: manual-to-manual, manual-to-automatic, automatic-to-manual, and automatic-to-automatic. Manual corresponds to operator or human intervention while automatic means machine only. The explanation that follows describes an automatic-to-automatic example.

After dialing, the calling unit, or originating fax, first transmits a calling tone (CNG) to indicate it is a non-speech terminal. The called unit, or answering fax, then responds with a called station ID (CED). The end of Phase A is signified after the called unit sends a 2100 Hz (CED) tone and the calling unit has detected this tone. Some facsimile manufacturers do not configure the modem to detect these tones. In this case, the modem looks for the preamble of flags (see phase B).

6.2.2 Phase B

The pre-message procedure consists of the following handshake. The answering fax machine sends an identification signal and the originating machine responds with a command signal. A training check is sent at a high speed and the receiving machine informs the transmitting machine if the training check was successful. This usually occurs at V.21 300 bps Frequency Shift Keying (FSK) modulation in HDLC format.

HDLC stands for High level Data Link Control. It is a standard procedure used for data communications. HDLC is a bit-oriented protocol (normally used in synchronous communications) that defines how the data being sent over the data link is organized and arranged.

When using the HDLC protocol, the data is transmitted via frames. These frames organize the data into a format specified by an ISO (International Standards Organization) standard that enables the transmitting and receiving station to synchronize with each other. Figure 6-20 illustrates the HDLC frame structure used for the facsimile protocol.

The preamble is a series of HDLC Flags for one second ±15%. The purpose of the 7E flags is to condition the line. The flag sequence defines the beginning and ending of a frame. The address field is required to provide identification for multi-point addressing. For PSTN the format is 11111111. The control field's purpose is to provide the capability of encoding the commands and responses. The format is 1100X000 (X = 0 non-final frame; X = 1 final frame).

The HDLC information field provides the specific information for the control and message interchange between the two stations. In the fax protocol the format for the information field consists of two parts, the Facsimile Control Field (FCF) and the Facsimile Information Field (FIF).

The FCF contains information regarding the type of information being exchanged and the position in the overall sequence. The acronyms, functions, and format for FCF commands are defined in the T.30 Recommendation. The FIF contains additional information which further clarifies the facsimile procedure. Some examples of information communicated with the

FIF are: group capability, data rate, vertical resolution, coding scheme, recording width, recording length, and minimum scan line time.

The Frame Check Sequence (FCS) follows the FIF. The modem automatically generate the FCS or Cyclic Redundancy Check (CRC). The frame ends with an ending 7E flag. It is recommended that more than one ending flag be transmitted.

After the modem has been configured for FSK, the Digital Identification Signal (DIS) is transmitted by the called unit. The DIS informs the calling unit about the called unit's capabilities such as group capability (G1, G2, G3), data rate, vertical resolution, coding scheme (Modified Huffman, Modified Read), recording width, recording length, and minimum scan line time. The calling unit then responds with a Digital Command Signal (DCS) which informs the called unit which options are chosen to complete this facsimile call.

After the DCS is transmitted, both the calling unit and the called unit set up for the high speed configuration that was chosen and transmitted via the DCS. A Training Check (TCF) is transmitted by the calling unit to verify training and give an indication of channel acceptability for the selected data rate. The TCF consists of a series of zeros for 1.5 seconds ±10%. Since the called unit knows it will be receiving 1.5 seconds of zeros, the host can make a decision whether the line is good enough at the chosen data rate or fallback to a slower speed.

After completing the TCF, the calling unit and the called unit re-configure for FSK, HDLC format. The called unit then transmits either a Confirmation to Receive (CFR) or a Failure To Train (FTT). The CFR is a response informing the calling unit of a successful pre-message procedure completion. A FTT informs the calling unit that the training signal was rejected and requests re-training. If a FTT is received by the calling unit, the fax protocol jumps back to the transition of DCS and continues until finally a CFR is received or the calling unit host decides to terminate the call.

6.2.3 Phase C

Phase C occurs after both facsimile machines have set up for the high speed configuration that was decided upon in phase B. The T.30 Error Correction Mode is addressed in a following section. The high speed message information is usually compressed data using a Modified Huffman (MH) or Modified Read (MR) algorithm. The host processor must perform the MH or MR compression before loading the data into the modem. On the receive end, the host processor must perform the MH or MR decompression.

The start of phase C is denoted by an End Of Line (EOL) 8-bit code. The data follows this first EOL character until the end of the line. Another EOL character is transmitted to indicate a new line. A minimum transmission time of a total coded scan line is measured from the beginning of the EOL to the beginning of the following EOL. If the transmitted data requires less time than the minimum transmission time, fill bits must be transmitted. Six consecutive EOL character constitute a Return To Control (RTC) command meaning end of document transmission. Figure 6-21 illustrates the phase C format.

6.2.4 Phase D

The post-message phase D procedure uses FSK and HDLC format. The calling station will typically send an End Of Message (EOM) signal. This FCF command (EOM) informs the called station that this is the end of the page and return to Phase B. A Multi-Page Signaling (MPS) or End Of Procedure (EOP) signal may be sent instead of EOM. The MPS signal informs the called unit that there are more pages in this facsimile transmission. EOP signals the end of the facsimile transmission. Procedure Interrupt-EOM (PRI-EOM), Procedure Interrupt-MPS (PRI-MPS), and Procedure Interrupt-EOP (PRI-EOP) indicate the same as EOM, MPS, and EOP, respectively, with the additional optional capability of requesting operator intervention. If operator intervention is required, further facsimile procedures commence at the beginning of phase B.

The called station might respond to an EOM, MPS, or EOP signal with a Message Confirmation (MCF) command. This FCF command indicates to the calling unit that the complete message was received. One of the following FCF commands may be sent instead of the MCF: Re-Train Positive (RTP), Re-Train Negative (RTN), Procedure Interrupt Positive (PIP), or Procedure Interrupt Negative (PIN). RTP indicates that a complete message has been received and that additional messages may follow after retransmission of TCF and CFR. RTN indicates that the previous message has not been satisfactorily received, however, further receptions may be possible provided there is a retransmission of TCF and CFR. PIP and PIN indicate that the previous message was received satisfactorily or not satisfactorily, respectively, and operator intervention is required for further transmissions.

6.2.5 Phase E

Call Release, or phase E, occurs after the last post-message signal of the procedure or under certain conditions such as a time-out, procedural interrupt, or a Disconnect (DCN) command.

The DCN command indicates the initiation of phase E. This command requires no response.

6.3 ERROR CORRECTION MODE

6.3.1 General

The T.30 contains an Error Correction Mode (ECM) option. The ECM allows the phase C portion of the facsimile transmission to be encoded in a HDLC framing format using a specified number of bits in the information field. The transmitted high speed message is broken up into a number of frames identified by frame numbers. If an error is detected during reception of the message, the called station records the frame number. After all the frames in the message has been received, the called station transmits the frame numbers that were received in error. The calling station then re-transmits only those frames in error. This continues until the entire message is received error free or the calling station decides not to transmit any more frames.

The error detection is performed by comparing the CRC or FCS. Using ECM, the fax data rate can be as fast as 14400 bps, therefore, the host microprocessor may not be able to keep up if implementing HDLC without the use of a serial I/O device.

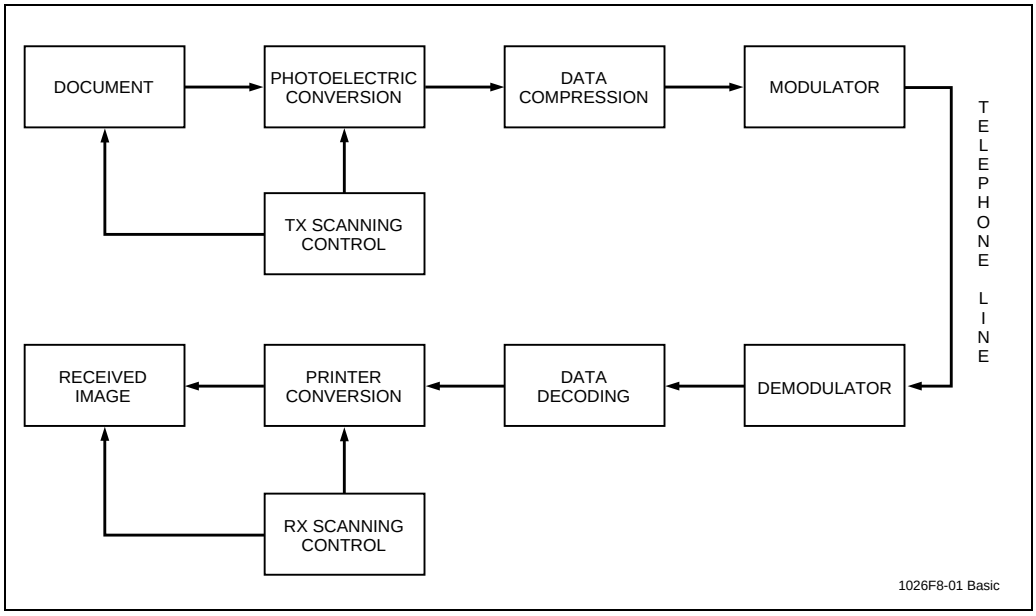


Figure 6-1. Basic Block Diagram of G3 Facsimile

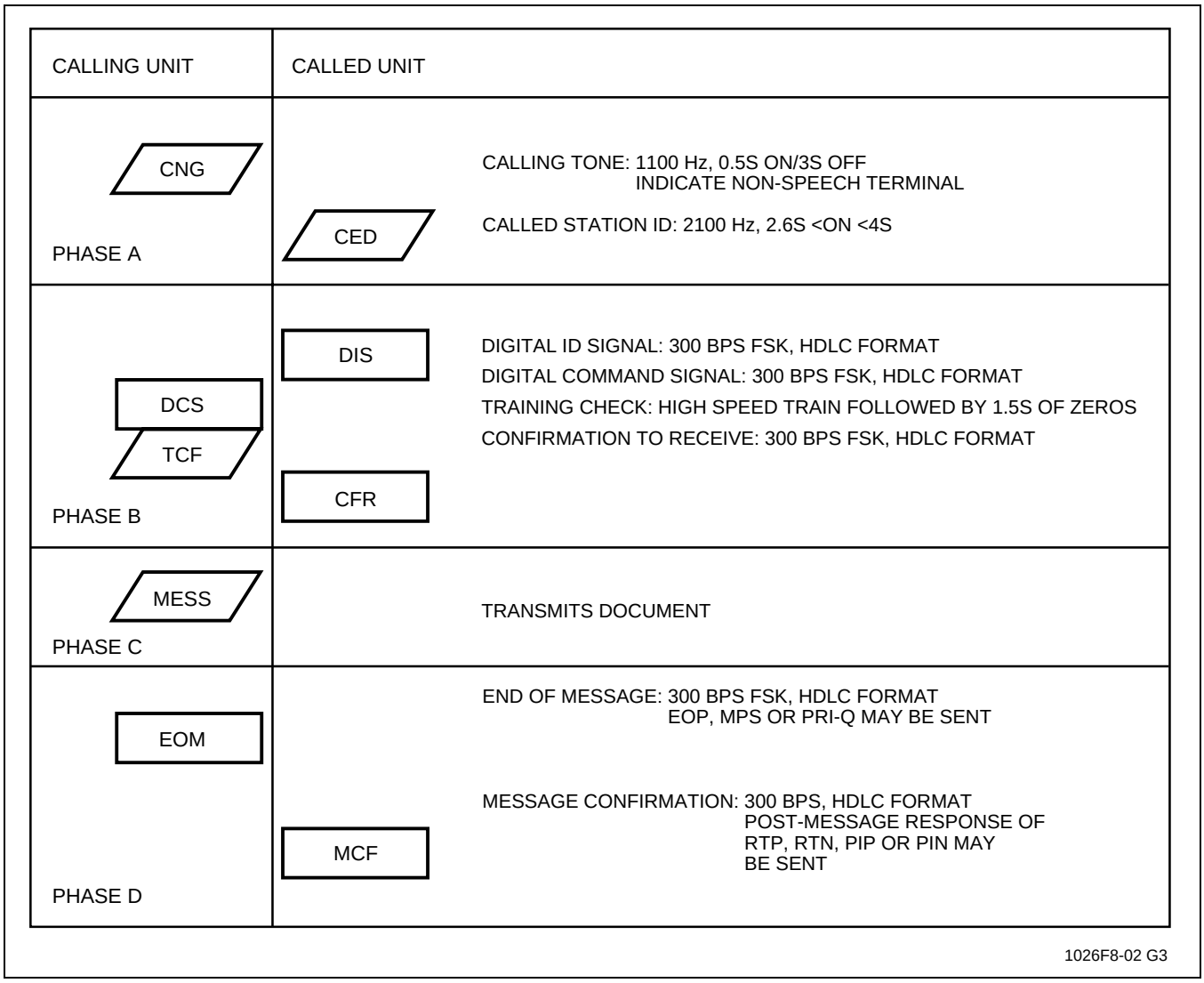


Figure 6-2. G3 Facsimile Procedure

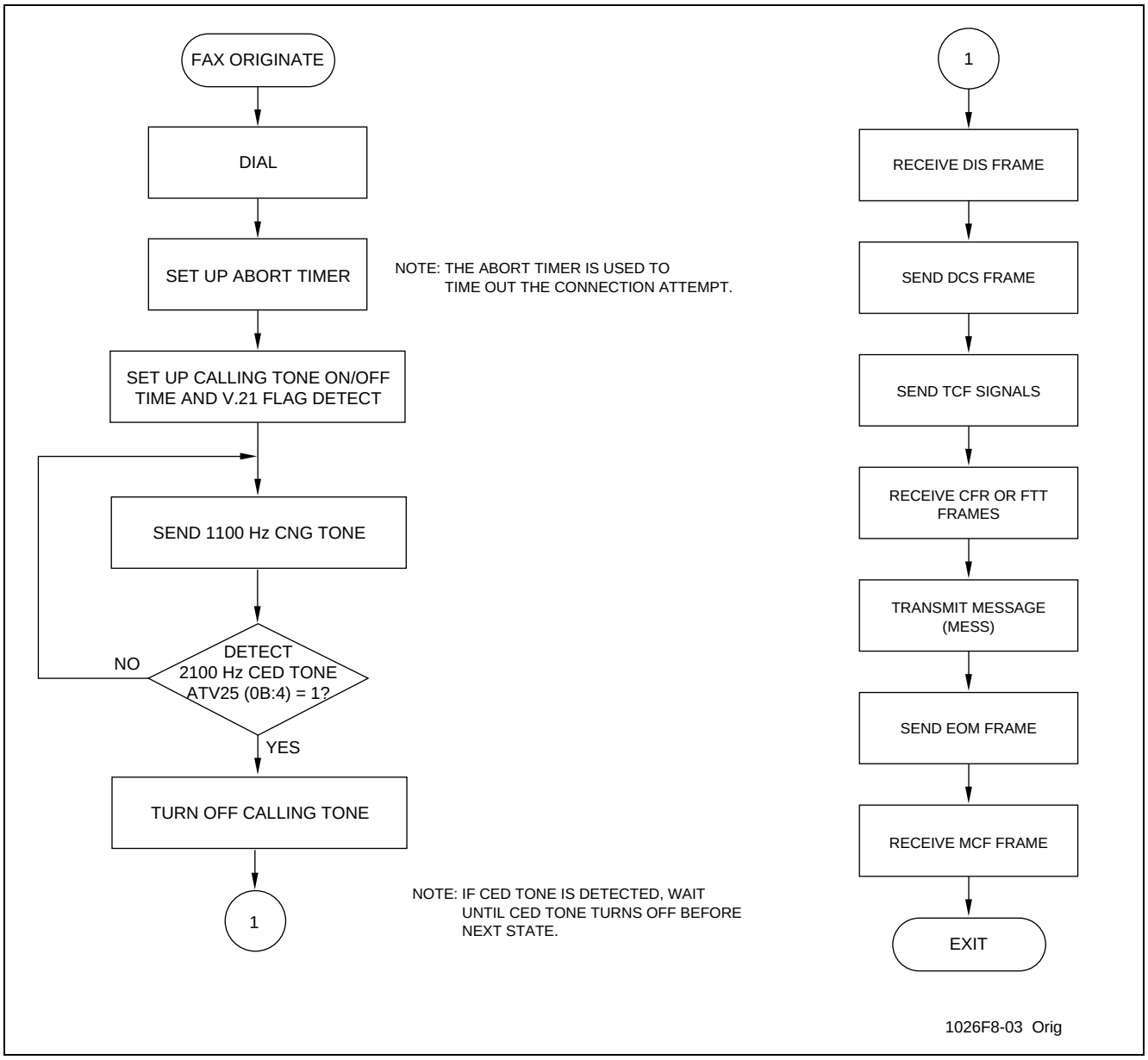


Figure 6-3. Originating a Fax Call - General

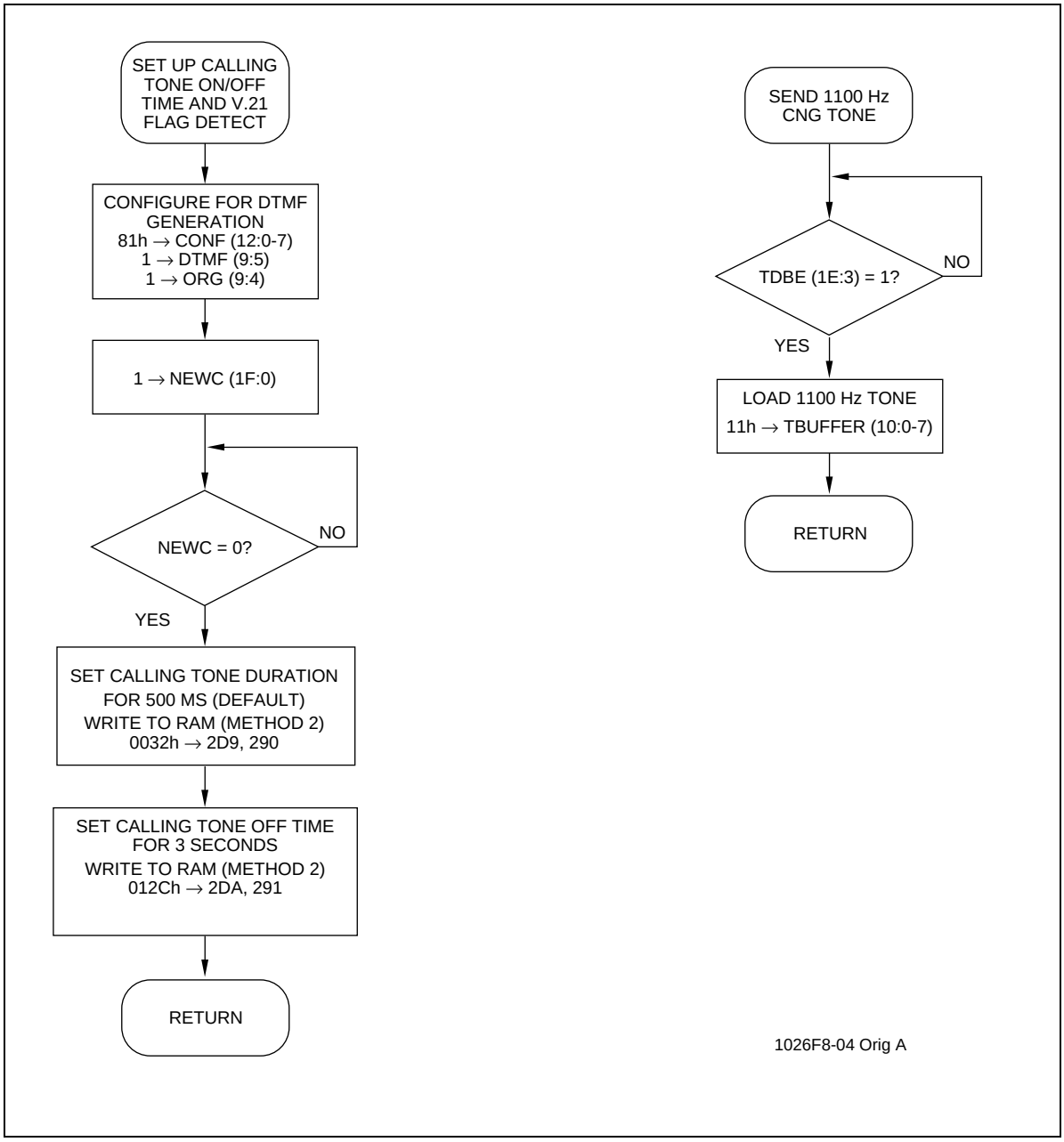


Figure 6-4. Originating a Fax Call - Phase A

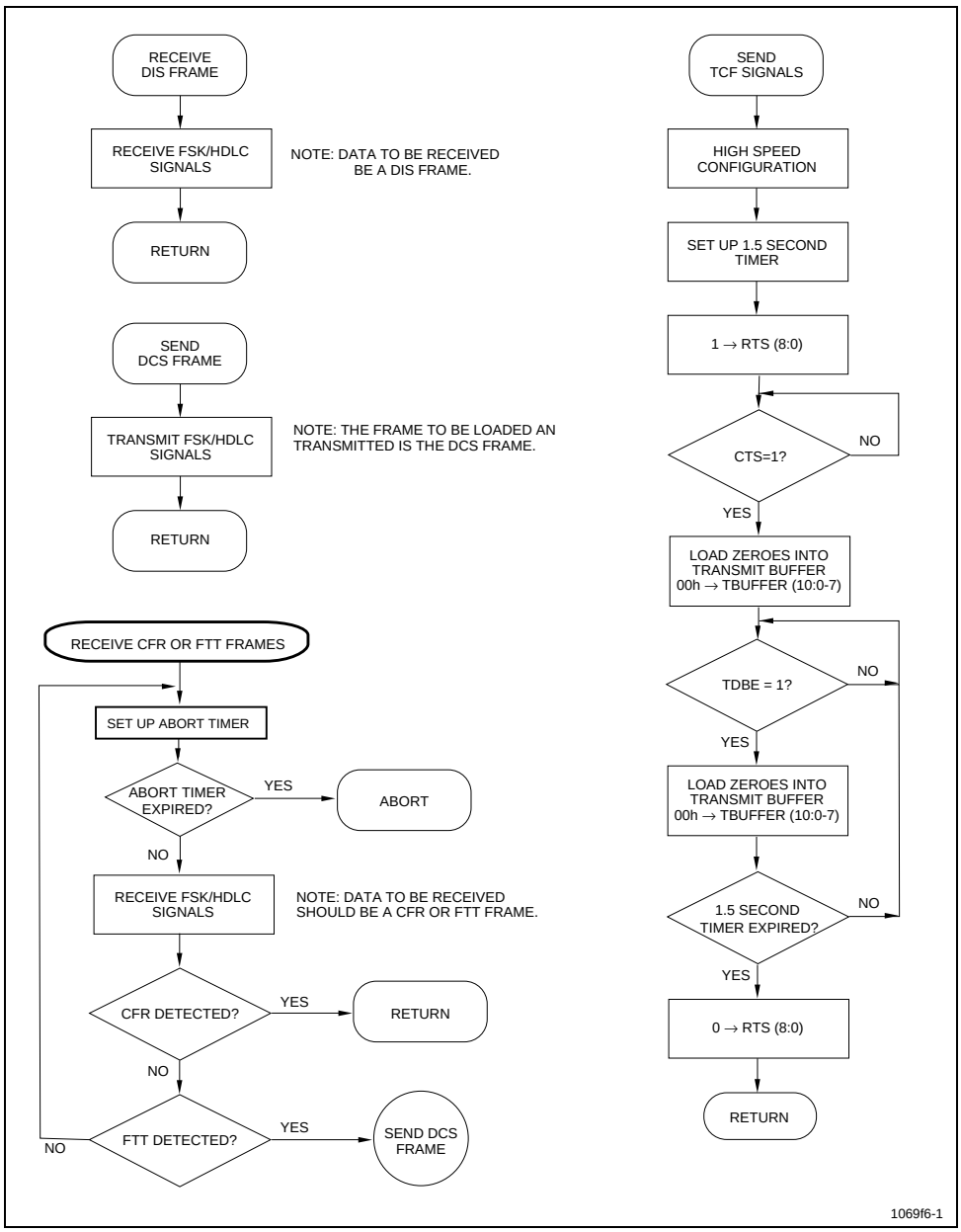


Figure 6-5. Originating a Fax Call - Phase B

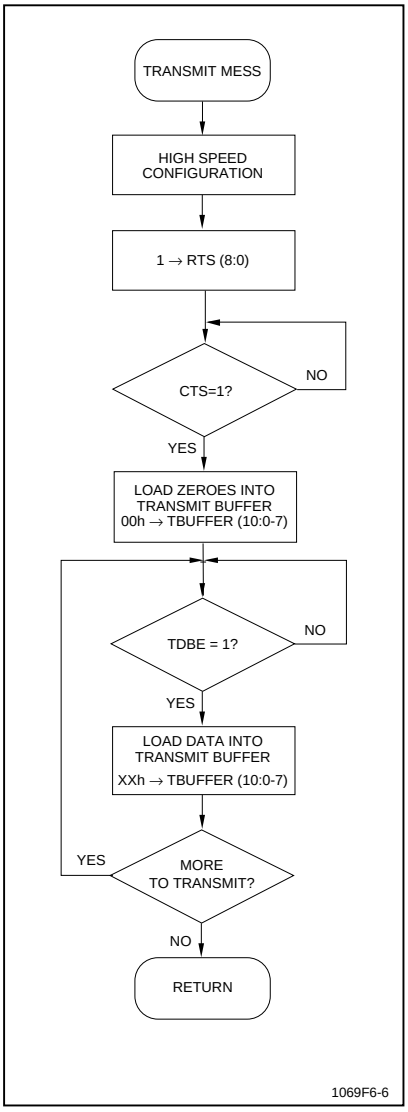


Figure 6-6. Originating a Fax Call - Phase C

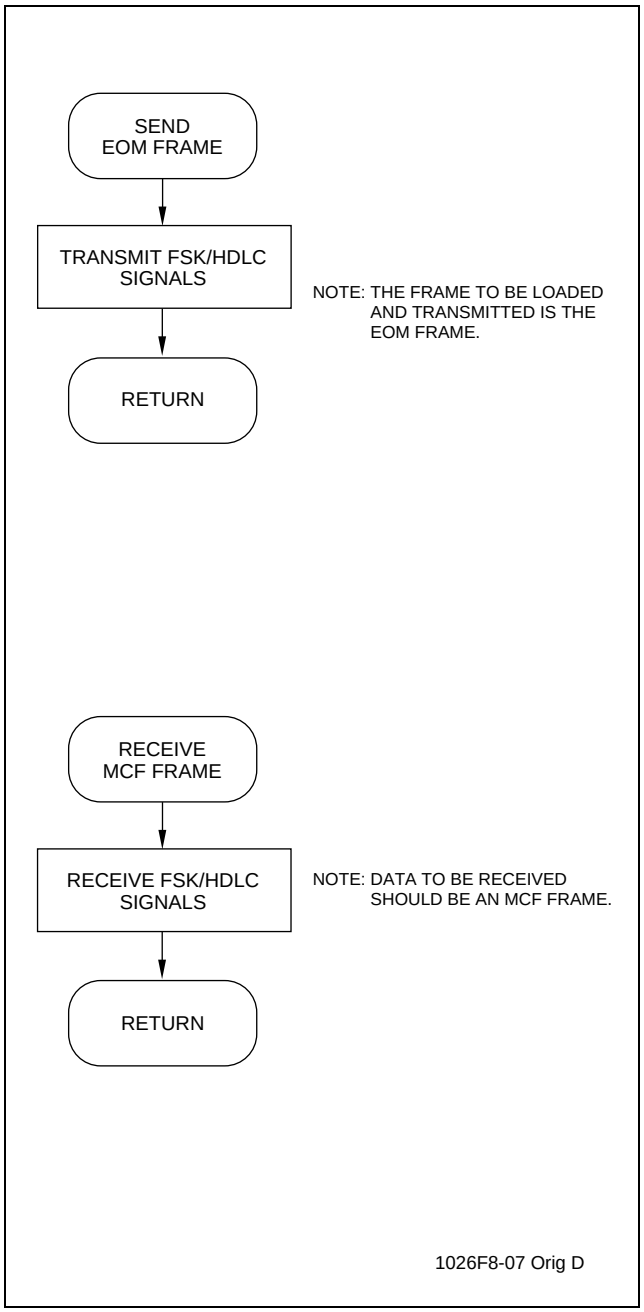


Figure 6-7. Originating a Fax Call - Phase D

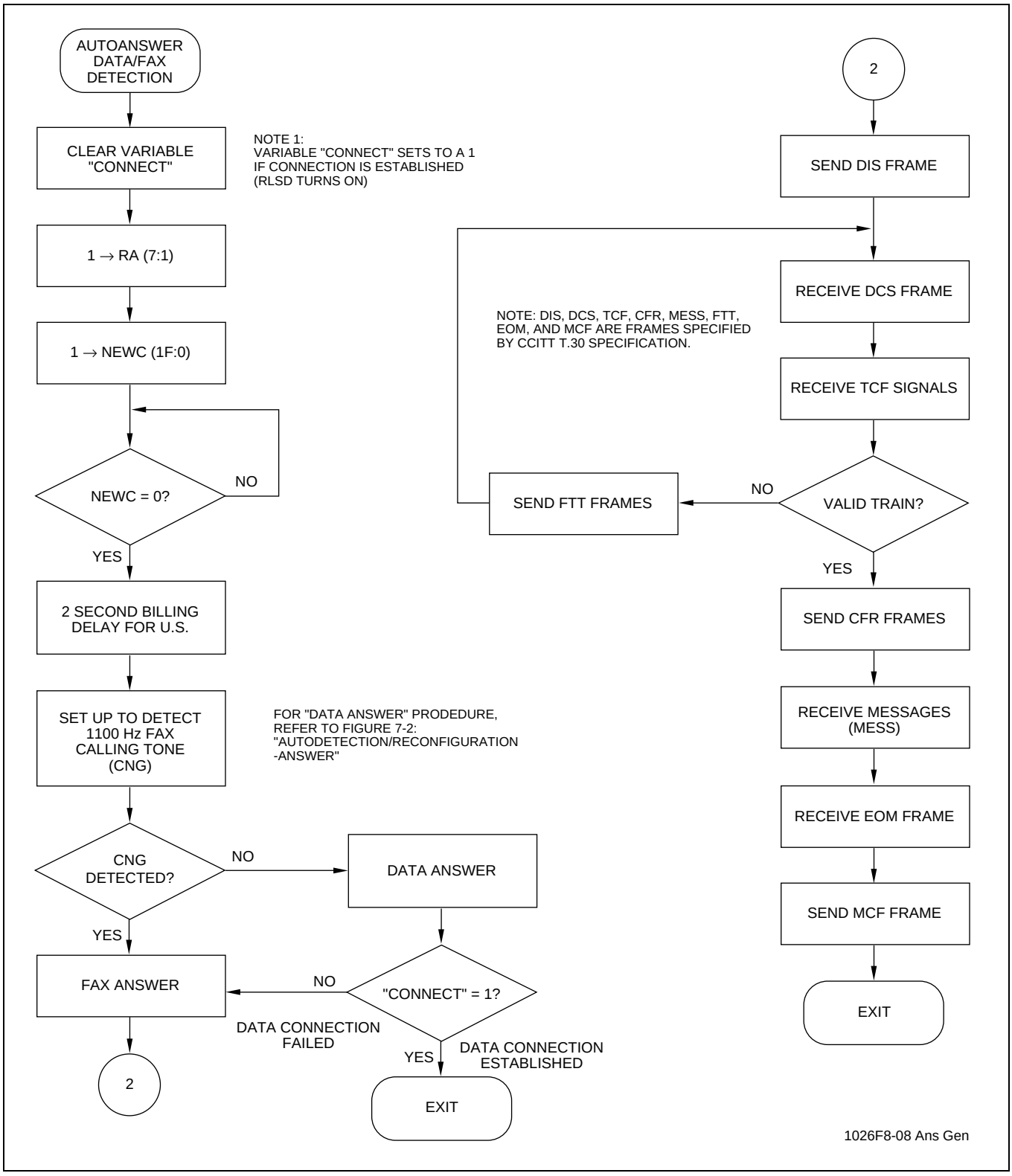


Figure 6-8. Answering a Fax Call - General

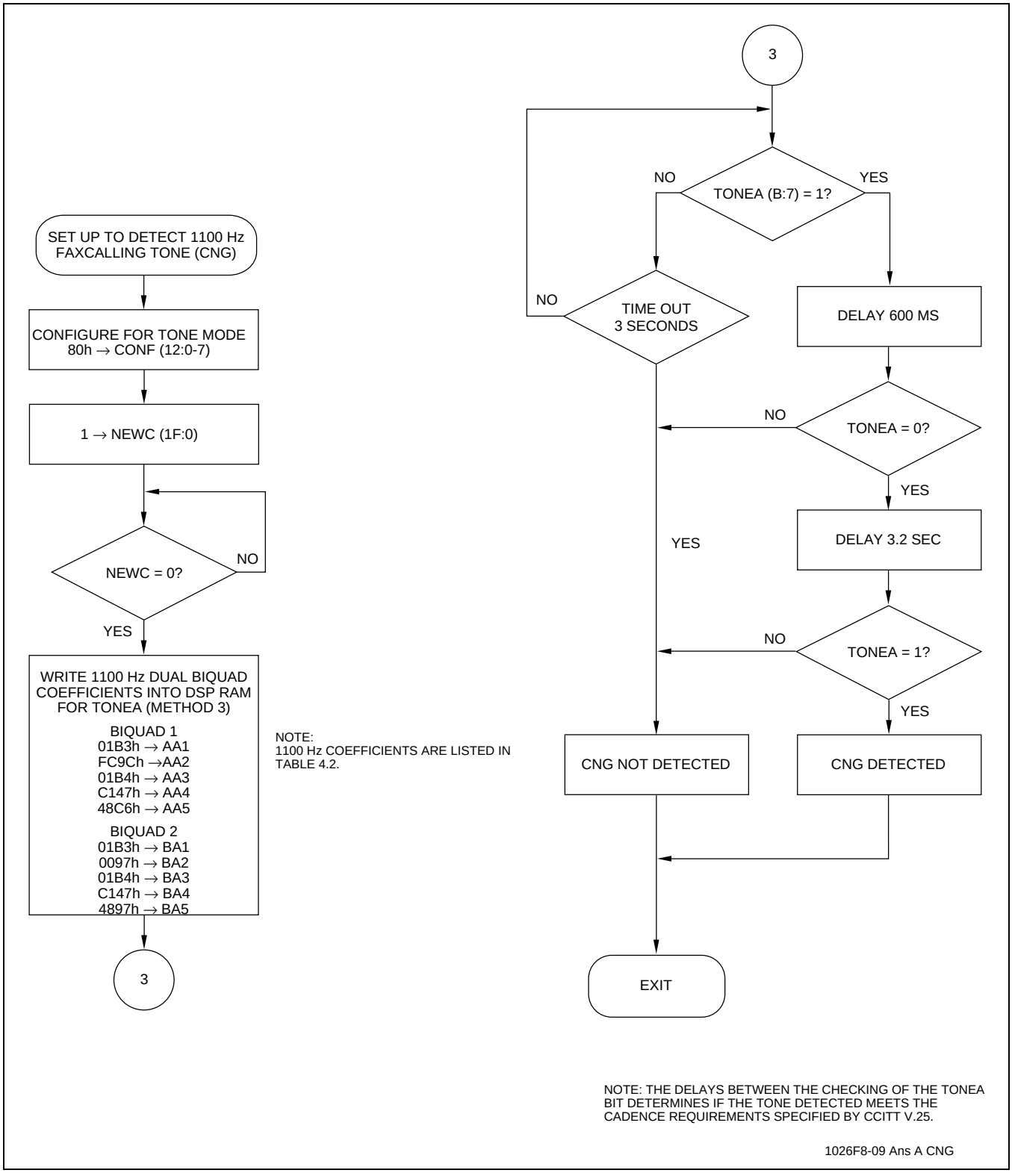


Figure 6-9. Answering a Fax Call - Phase A (CNG)

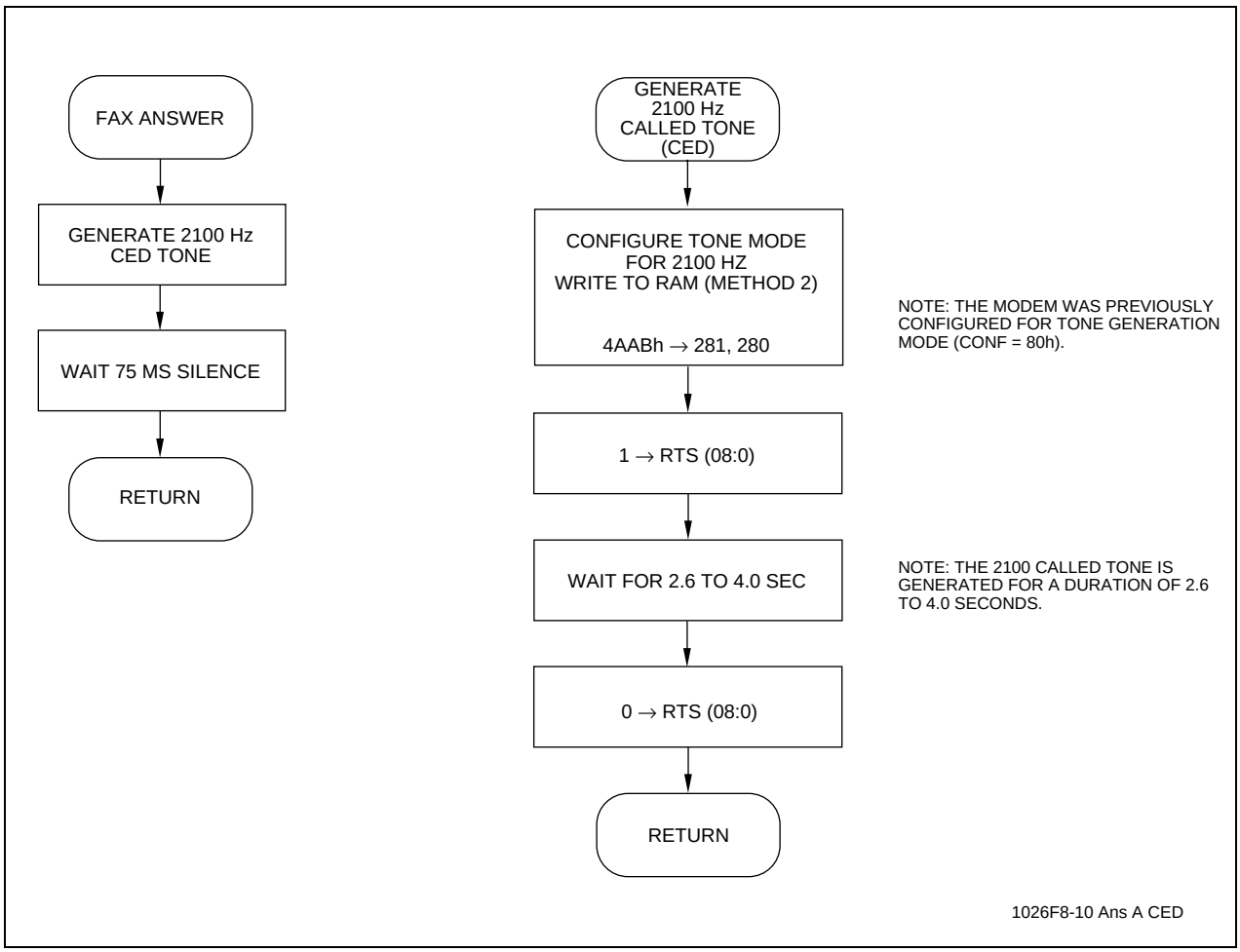


Figure 6-10. Answering a Fax Call - Phase A (CED)

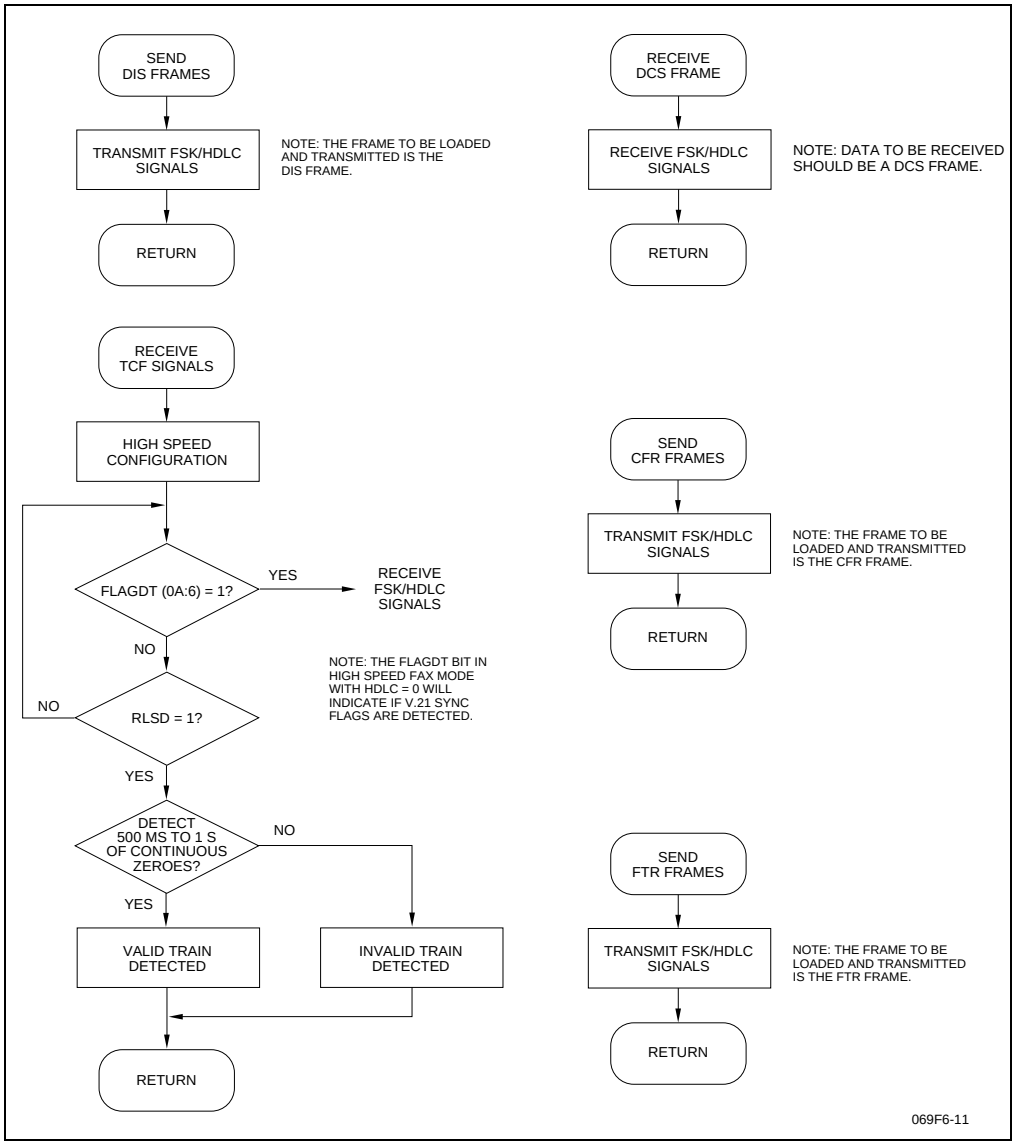


Figure 6-11. Answering a Fax Call - Phase B

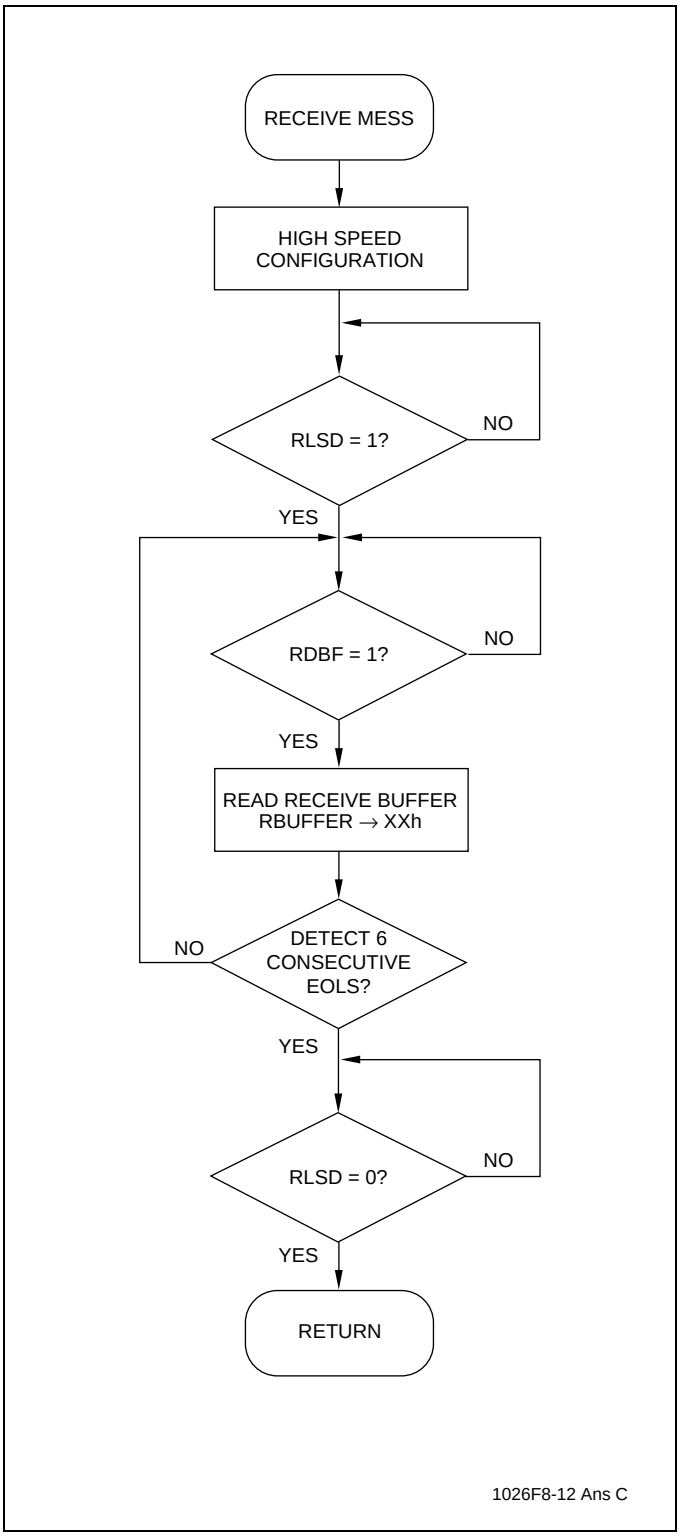


Figure 6-12. Answering a Fax Call - Phase C

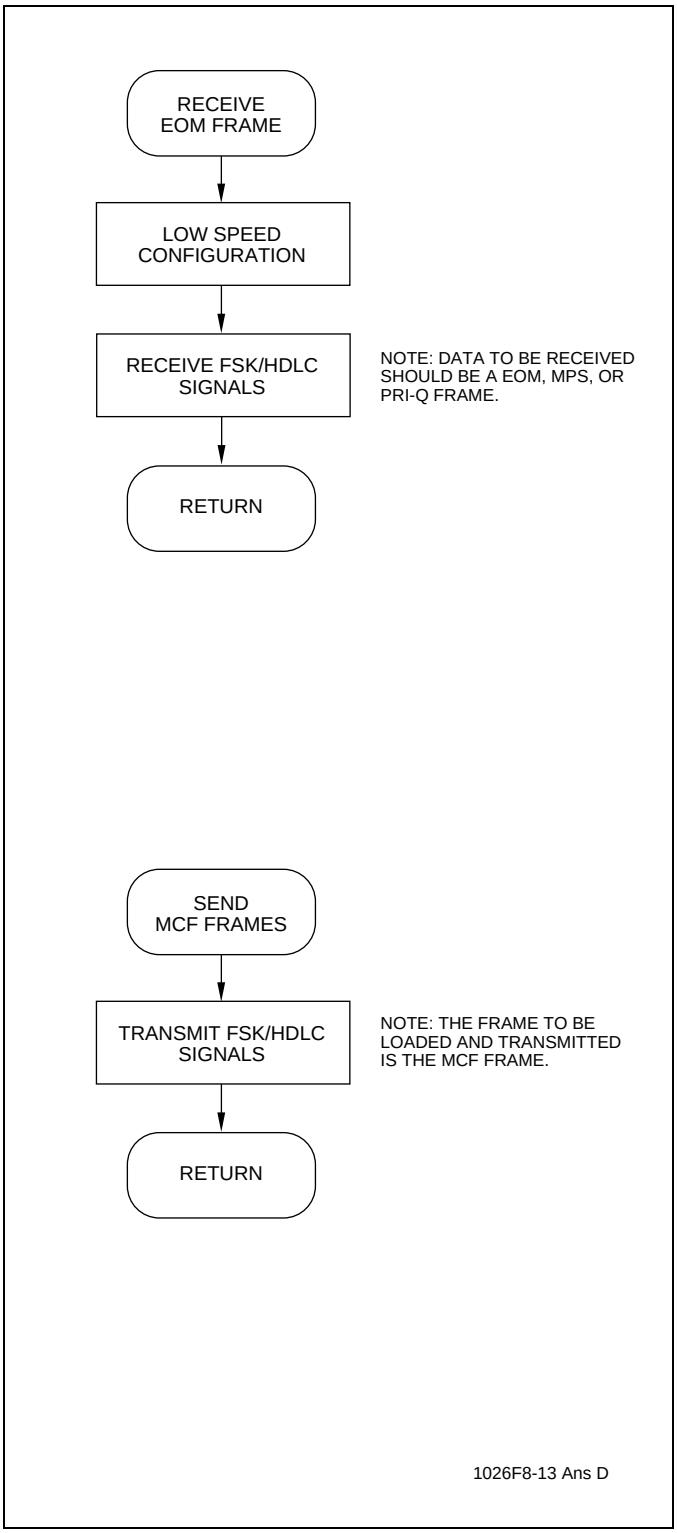


Figure 6-13. Answering a Fax Call - Phase D

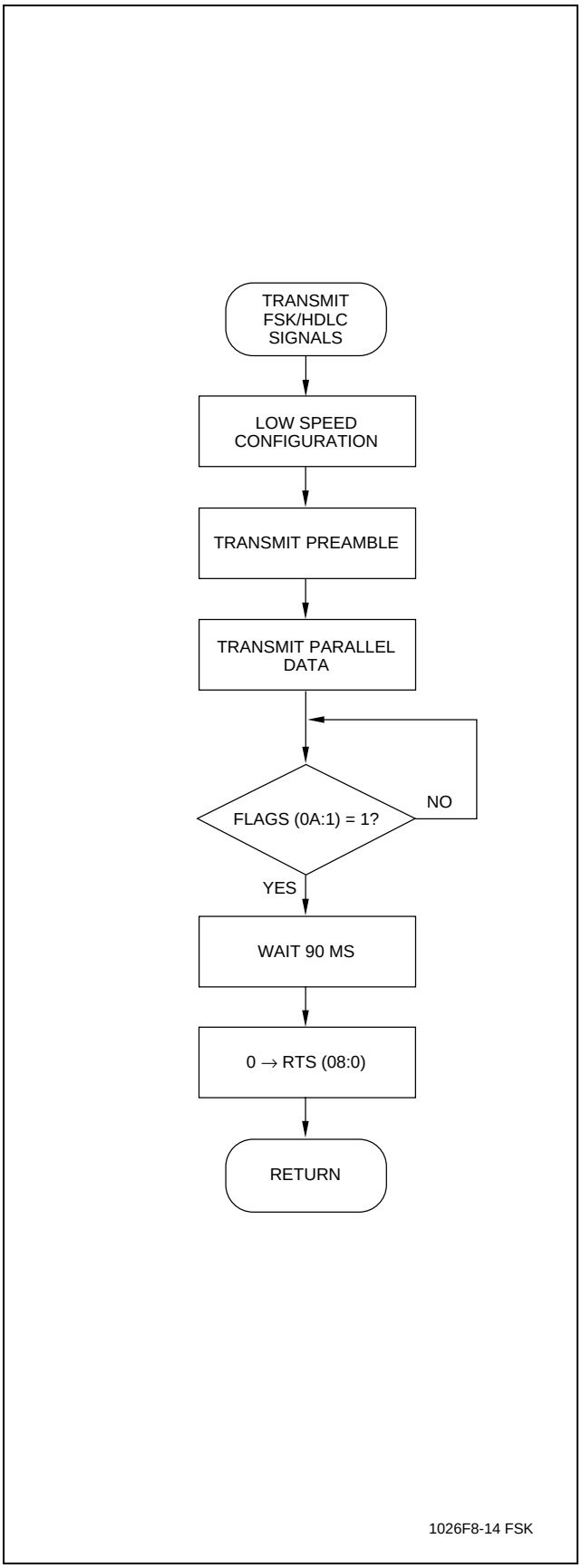


Figure 6-14. Transmitting FSK/HDLC Signals

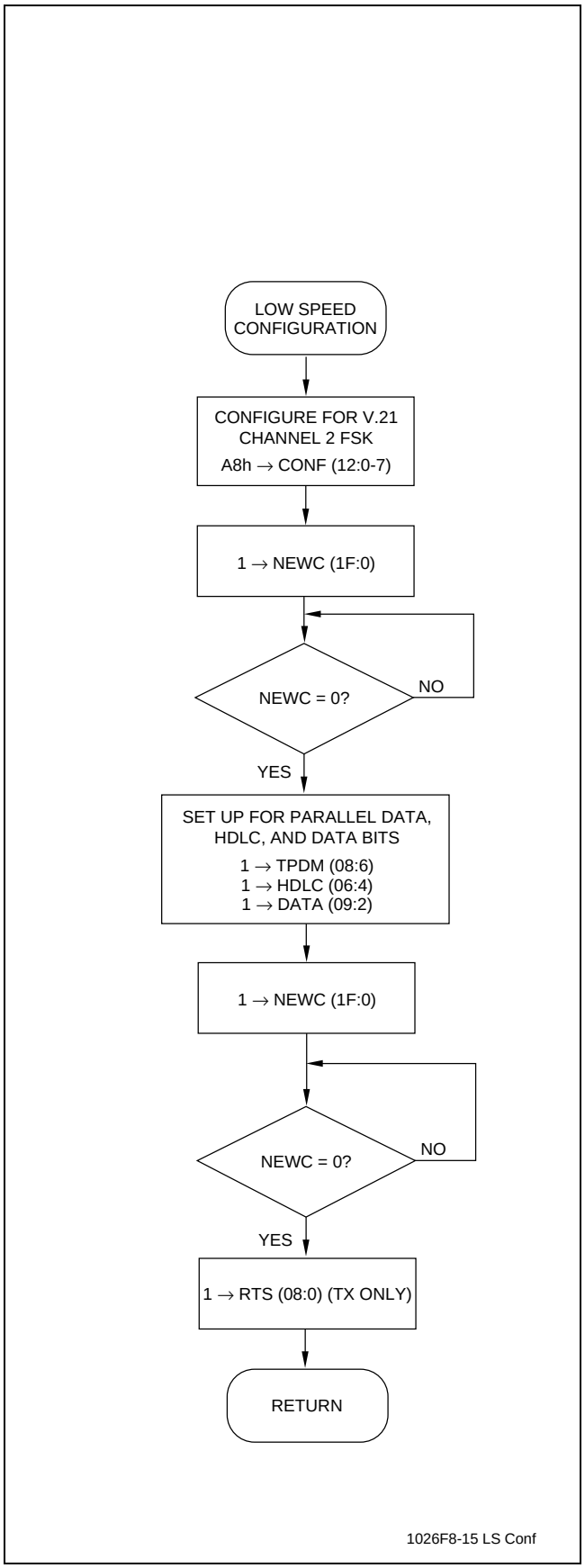


Figure 6-15. Low Speed Configuration Routine

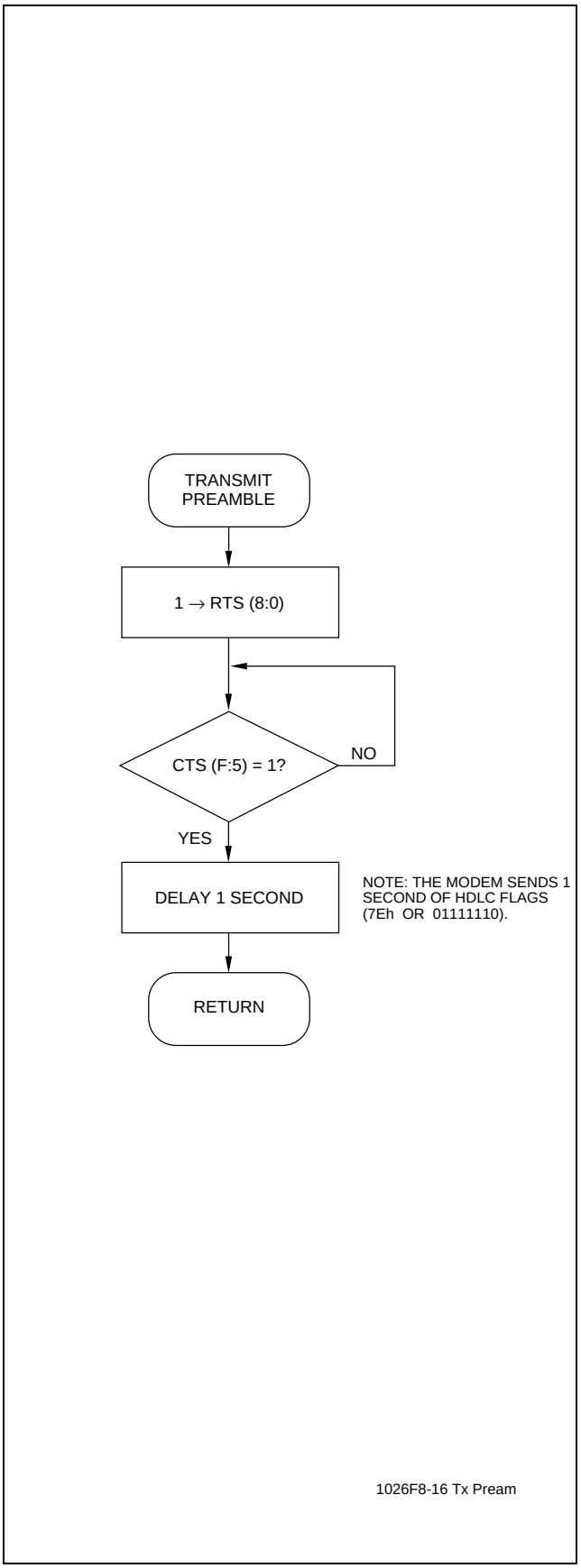


Figure 6-16. Transmit Preamble Routine

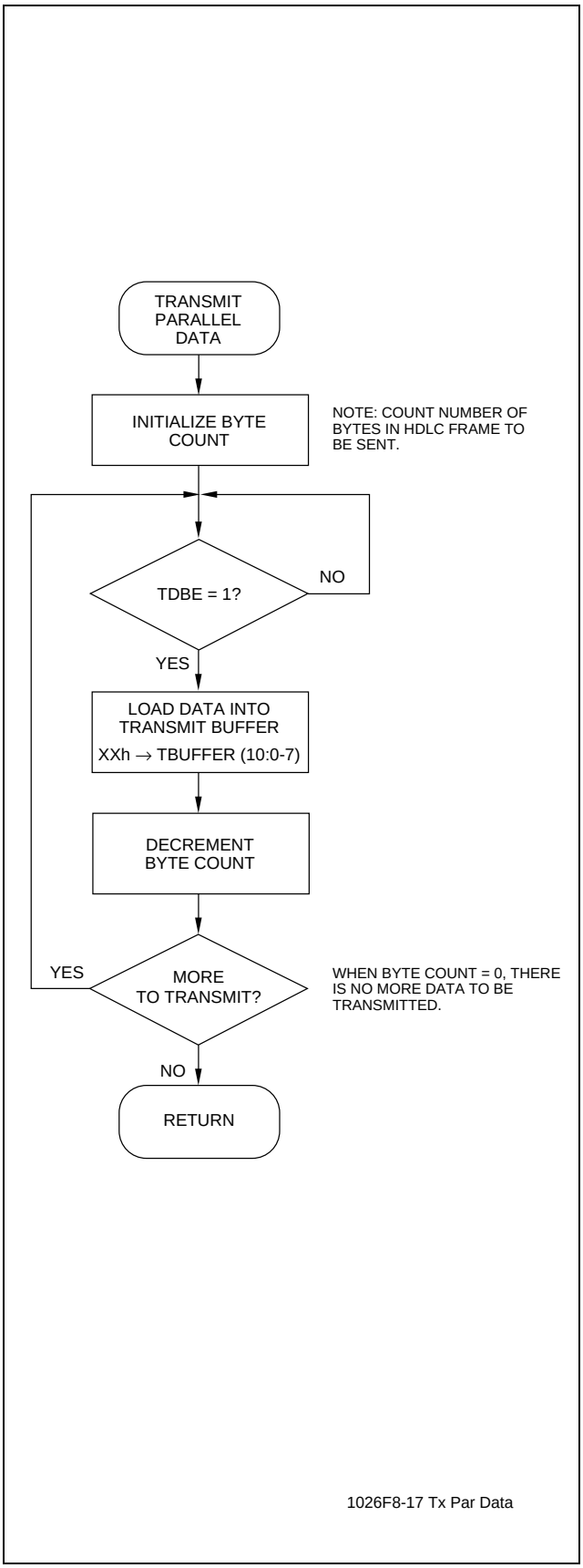


Figure 6-17. Transmit Parallel Data Routine

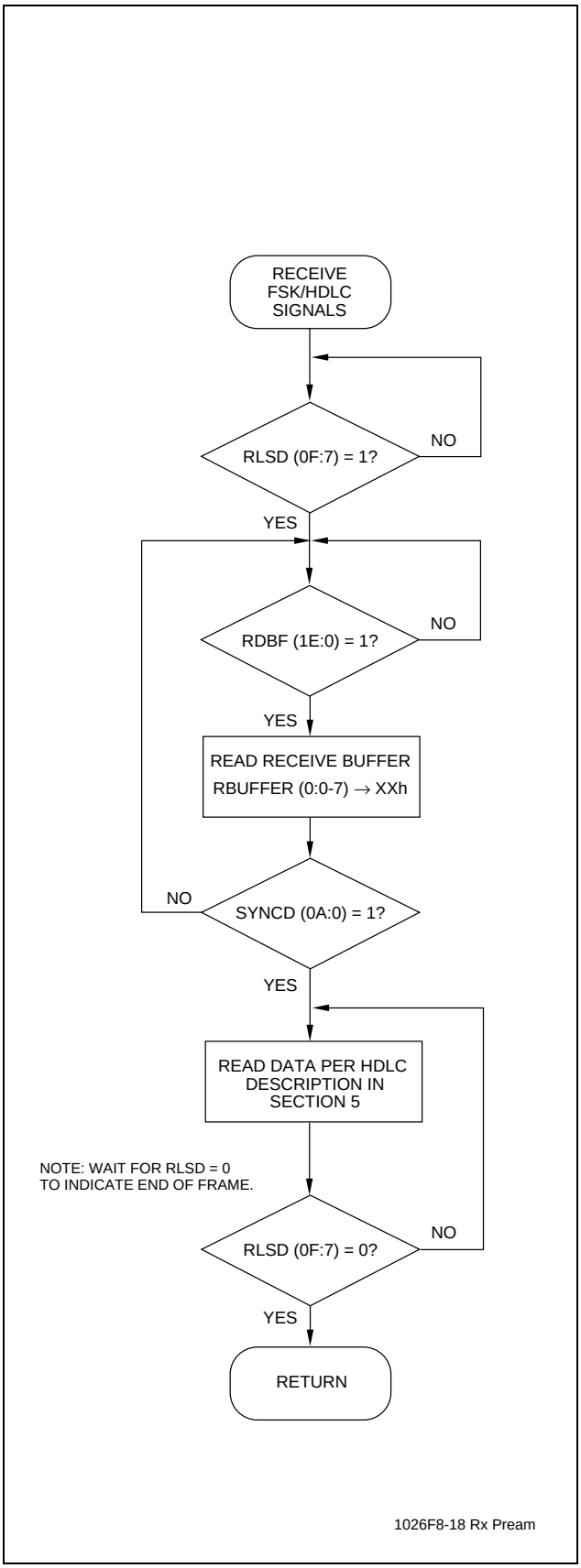


Figure 6-18. Receive FSK/HDLC Signals

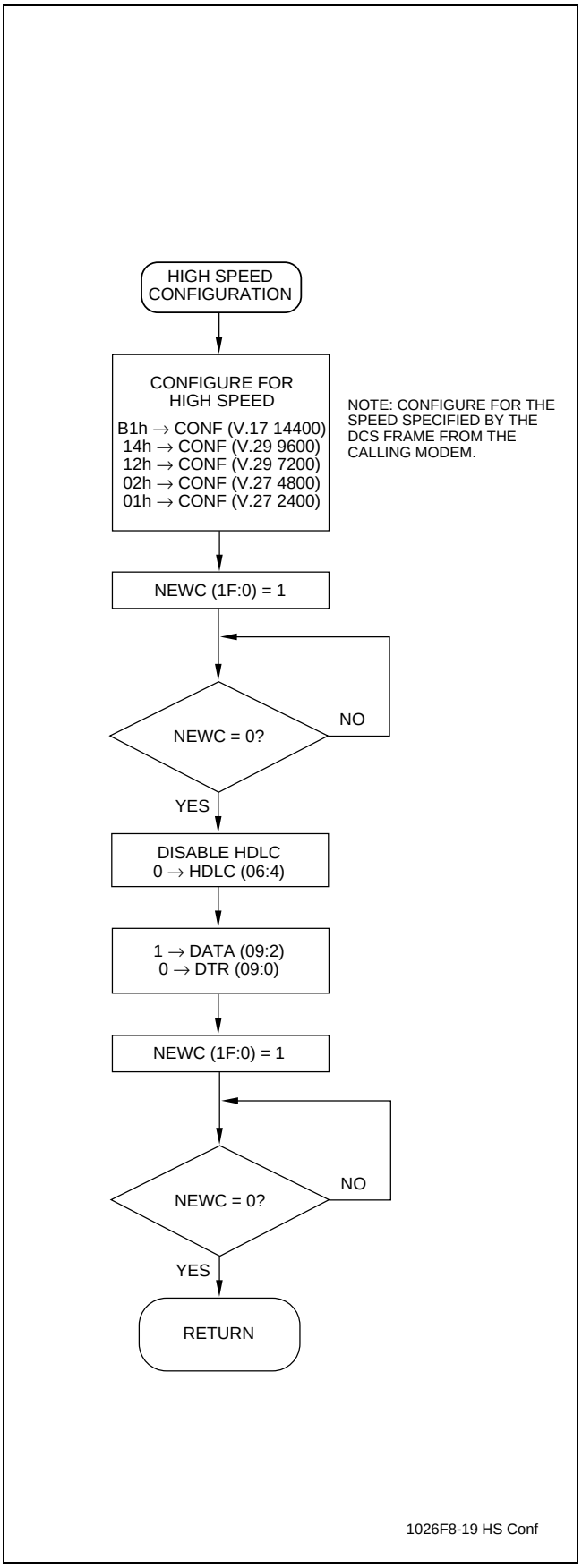


Figure 6-19. High Speed Configuration Routine

6.3.2 ECM Frame Structure

In Error Correction Mode, one frame of facsimile data consists of 256 or 64 octets of data. Each page may contain 1 to 256 frames. Also, 1 to 256 pages may be transmitted. The ECM frame structure is illustrated in Figure 6-22. Following the high speed training sequence, the flag, address field, and control field is transmitted. In ECM, Flag = 7E, Address = FF, and Control = B0. The Facsimile Control Field for the Facsimile Coded Data block (FCD) is 60. The frame number follows the FCF for FCD, followed by the facsimile data. Pad bits such as EOL, Tag, and Align bits follow the facsimile data. Finally, the FCS check and the ending flag is transmitted.

After 256 frames, a Return Control for Partial page (RCP) block is transmitted three times. The RCP block consists of the same Flag, Address Field, and Control field followed by the FCF for RCP. The FCS immediately follows with the ending flag. After the third RCP, a maximum of 50 ms of flags are transmitted.

An ECM message protocol example is shown in Figure 6-23. The bold arrows are high speed transmissions and the other arrows are FSK transmissions. The example is self-explanatory. If more information is needed, refer to the T.30 ECM specification.

In this paragraph, the Q refers to the NULL, EOP, MPS, or EOM Facsimile Control Field commands. The Partial Page Signals (PPS-Q) and Partial Page Request (PPR) frame structures are shown in Figure 6-24. The PPS-Q frame begins with the same Flag, Address field, and Control field. Two FCF commands follow. The first FCF transmitted is to indicate PPS. The second FCF is either NULL, EOP, MPS, or EOM. The page count followed by the block count, followed by the total number of frames in the block are transmitted next. The FCS and ending flag are finally transmitted.

The PPR frame structure also begins with the same Flag, Address, and Control field. The FCF for PPR is the next octet. The FIF consists of 256 or 64 bits depending on how many frames were transmitted. The contents of FIF is either a 0 or a 1. The bit number corresponds to the frame number and a 0 indicates the frames was received correctly and a 1 indicates an incorrect frame was received.

6.4 SIGNAL RECOGNITION ALGORITHM

A method of determining whether a high speed message or FSK handshaking is being received by the modem is necessary when implementing the T.30 recommendation. When the calling unit transmitter and called unit receiver configure for V.29 or V.27 ter, sometimes the high speed message may not be received (typically due to a noisy line). In this case, the calling unit transmitter will try to send the message up to three times before re-negotiating in FSK signaling. The called unit receiver must, therefore, be able to distinguish between a high speed message and FSK handshaking.

The algorithm shown in Figure 6-25 can be used to perform the signal recognition. The use of the P2DET and PNDET status bits may also be incorporated for qualifying high speed PSK carrier.

High speed PSK reception in high noise environments can be optimized by setting the RTH bits so that the level of the noise is below the modem's receiver threshold. This can be accomplished by measuring the received signal level via the AGC gain word RAM access while receiving the V.21 channel 2 carrier. Then, after configuring to a high speed configuration, RTH should be set to a value which will provide a threshold range centered around the expected receive level.

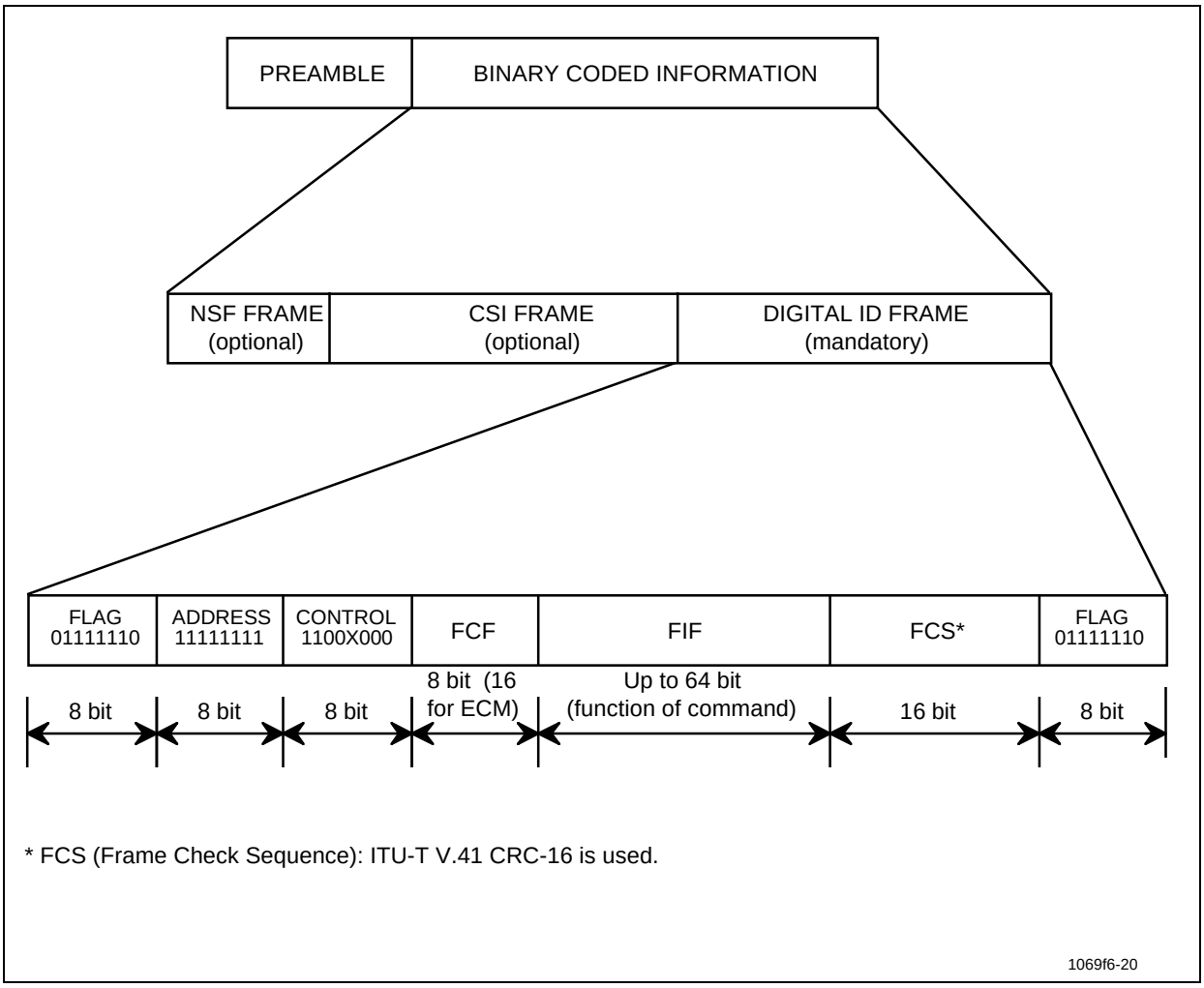


Figure 6-20. HDLC Frame Structure

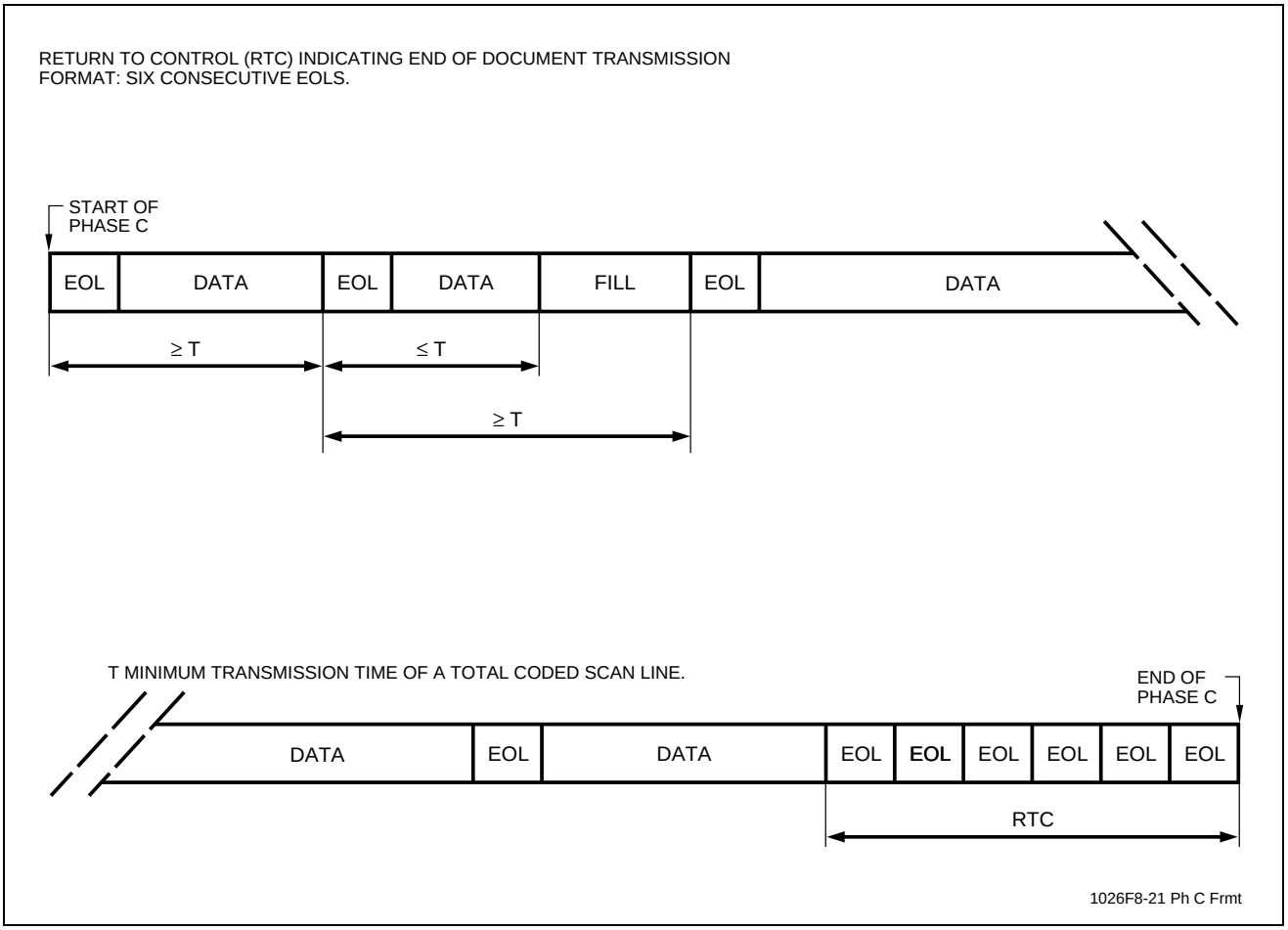


Figure 6-21. Phase C Format

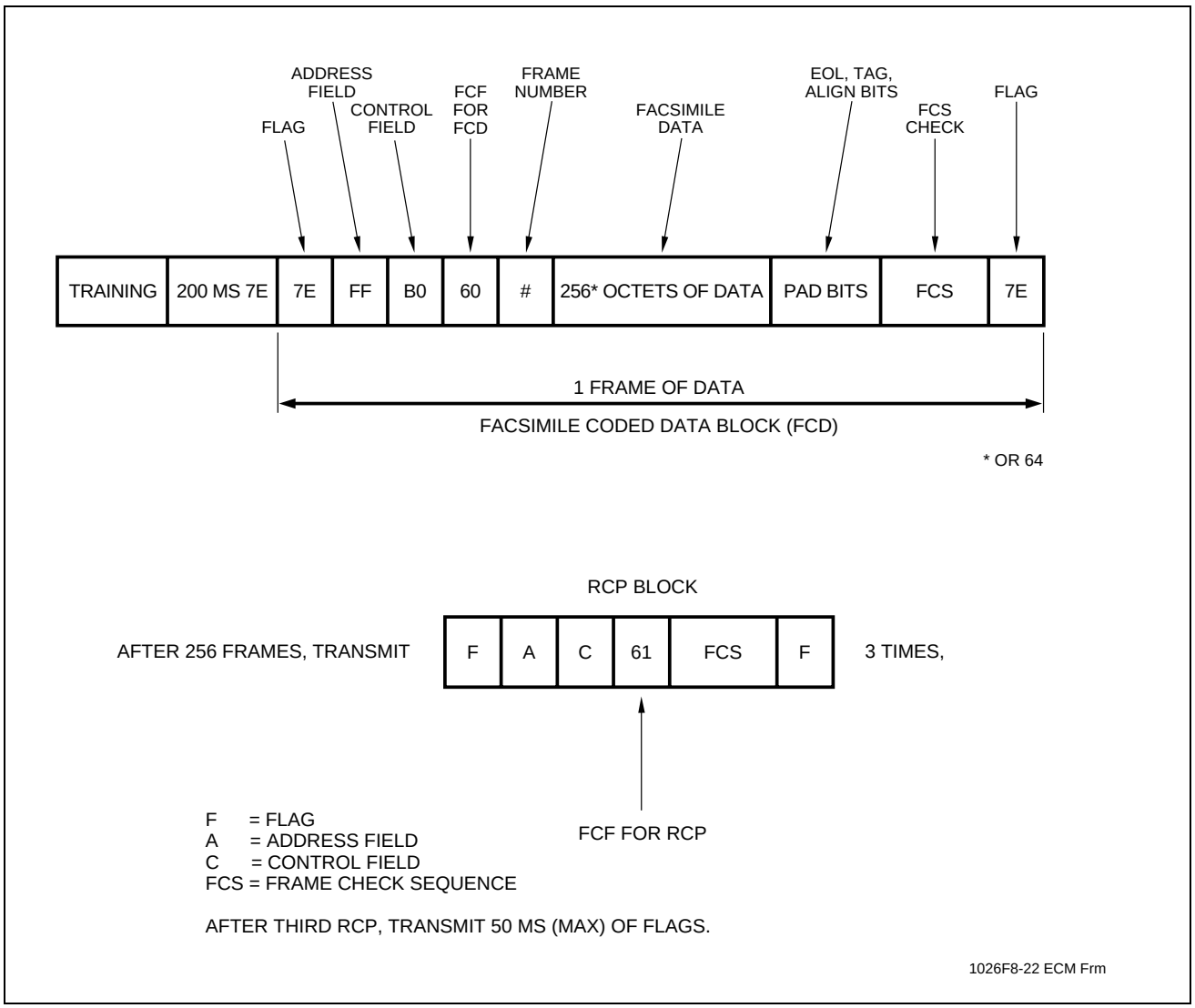


Figure 6-22. ECM Frame Structure

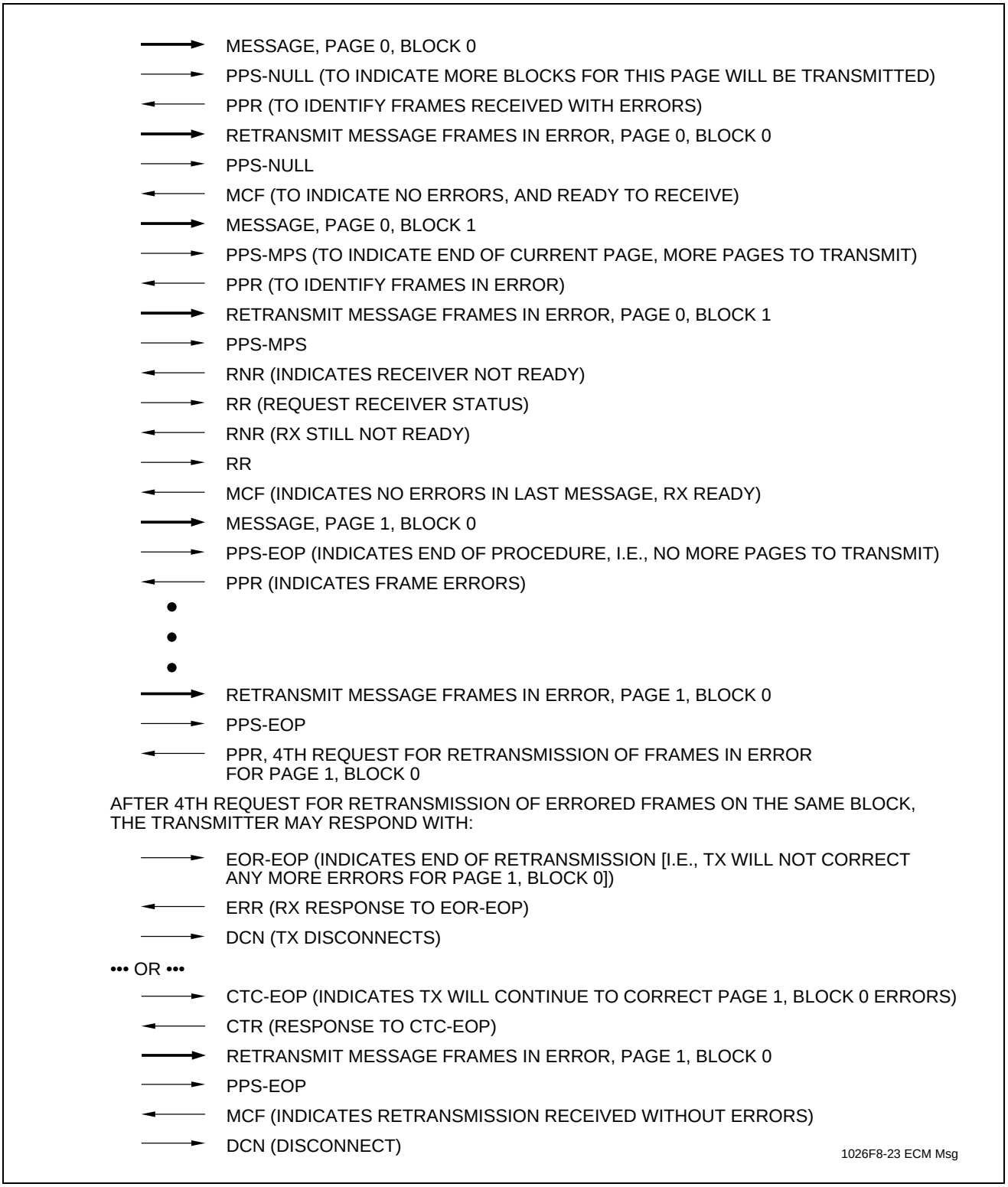


Figure 6-23. ECM Message Protocol Example

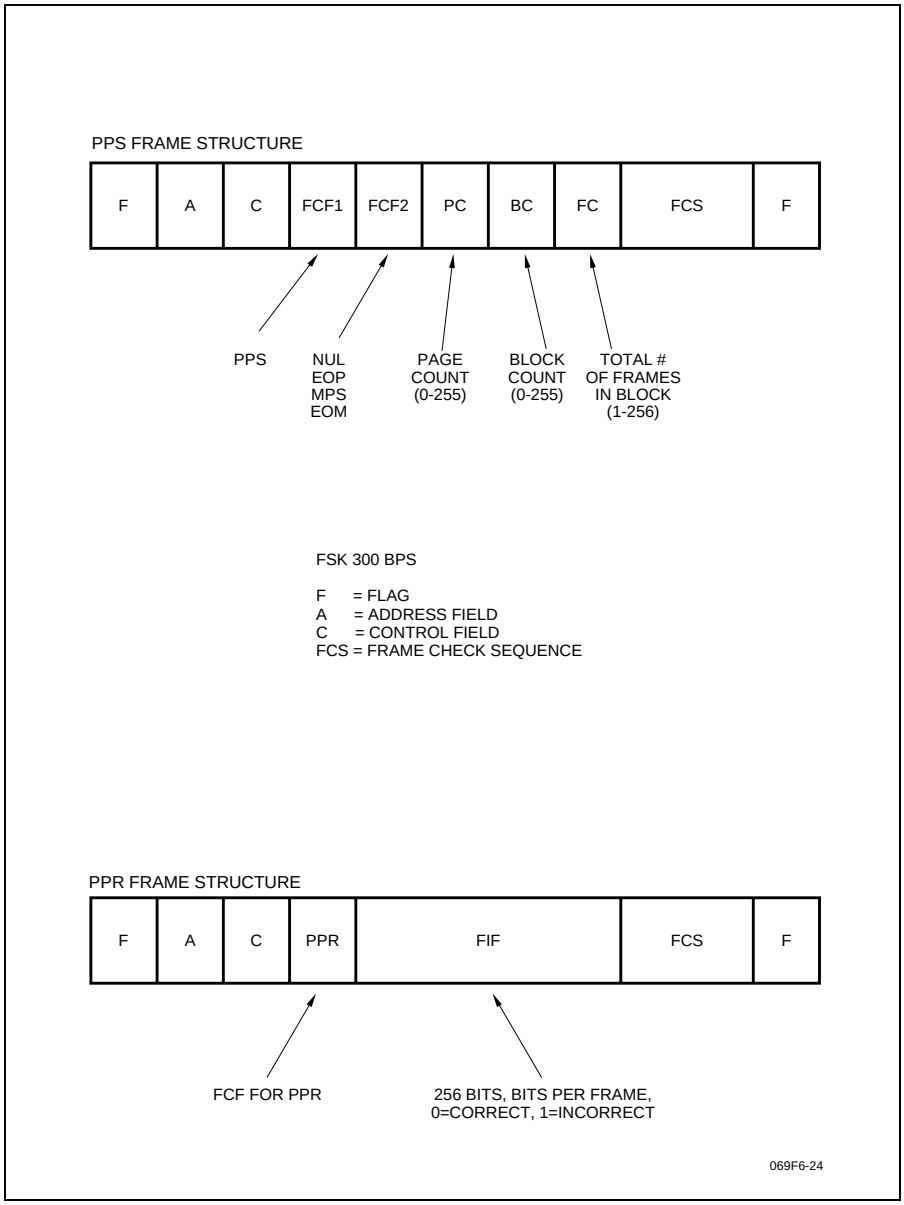


Figure 6-24. PPS and PPR Frame Structure

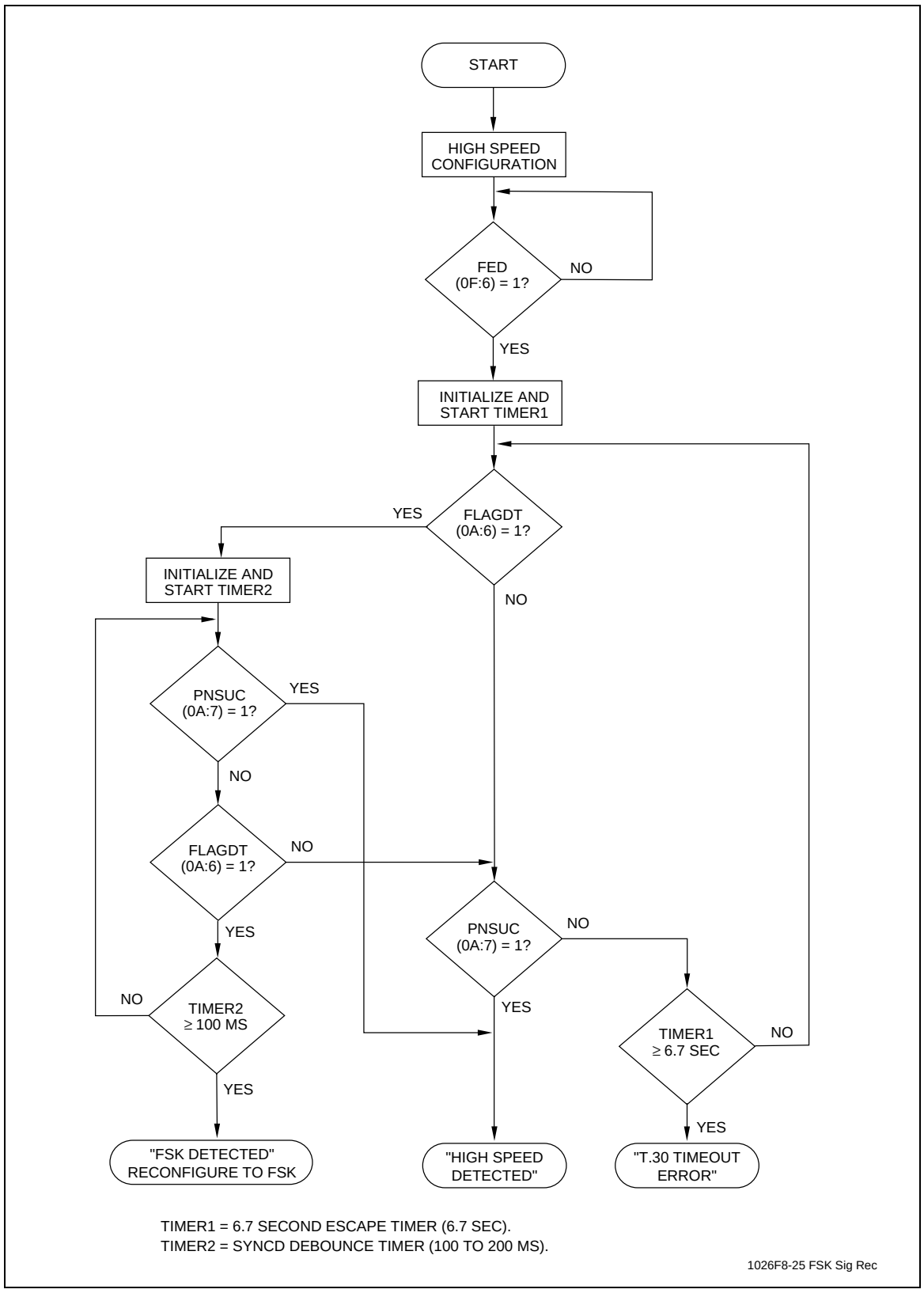


Figure 6-25. FSK Signal Recognition Algorithm

7. V34FAX OPERATION CONSIDERATIONS

This chapter discusses the operation of V34FAX, considering both the original V.21 procedures and the new ITU-T Recommendation V.8 (hereafter V.8) based startup procedure. V.21/V.8 interoperability and the related topic, turnaround polling, are also described.

Section 7.1 discusses the theory of V34FAX half-duplex operations defined in ITU-T Recommendation V.34 (section 12), Recommendation V.8, and Annex F to Recommendation T.30.

Section 7.2 summarizes the various start-up scenarios for fax including: automatic start, manual start, and missed signals. The scenarios are described and the associated detectors needed at each stage are identified. Section 7.3 discusses turnaround polling scenarios. Section 7.4 is a summary of all detectors active during a given state of operations

Sections 7.5 and 7.6 include descriptions of the modem operations during startup and turnaround polling, including handshake monitoring.

7.1 V.34FAX Operation Specifications

The V.34FAX half-duplex operation is a mode of operation wherein exchange of data alternates between unidirectional transmission of primary channel data (from source to recipient modem), and simultaneous bi-directional transmission of control channel data. The revised ITU-T Recommendation T.30 describes the procedures for the optional use of the half-duplex V.34 modulation system.

The V.34 half-duplex mode is used for data transmission; the duplex control channel is used in pseudo half-duplex to provide binary coded procedural data and to replace the original V.21 Channel 2. The use of ECM mode is mandatory for all facsimile messages using the V.34 modulation system. Figure 7-1 shows a typical V.34FAX starting sequence of events.

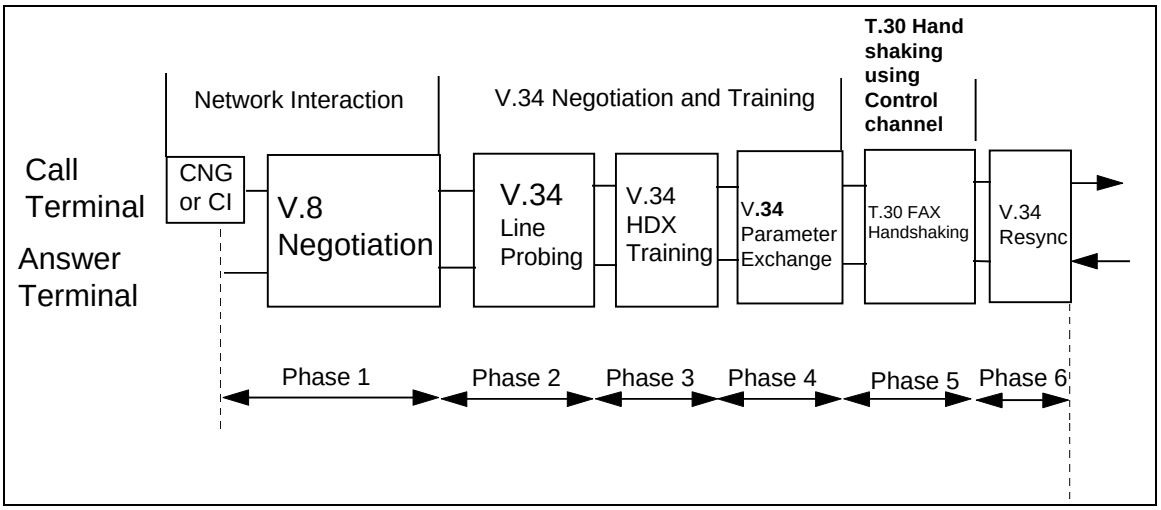


Figure 7-1. V34FAX Starting Sequence

In Phase 1 the new V.8 defined procedures are used for the network interaction and provide initial negotiations between two modems. Using V.21 modulation both modems provide the information on the Call function, the protocol available, the network access, and the modulation modes available.

Figure 7-2 shows the Phase 1 exchange. In Phase 2 modems perform a channel probing and ranging.

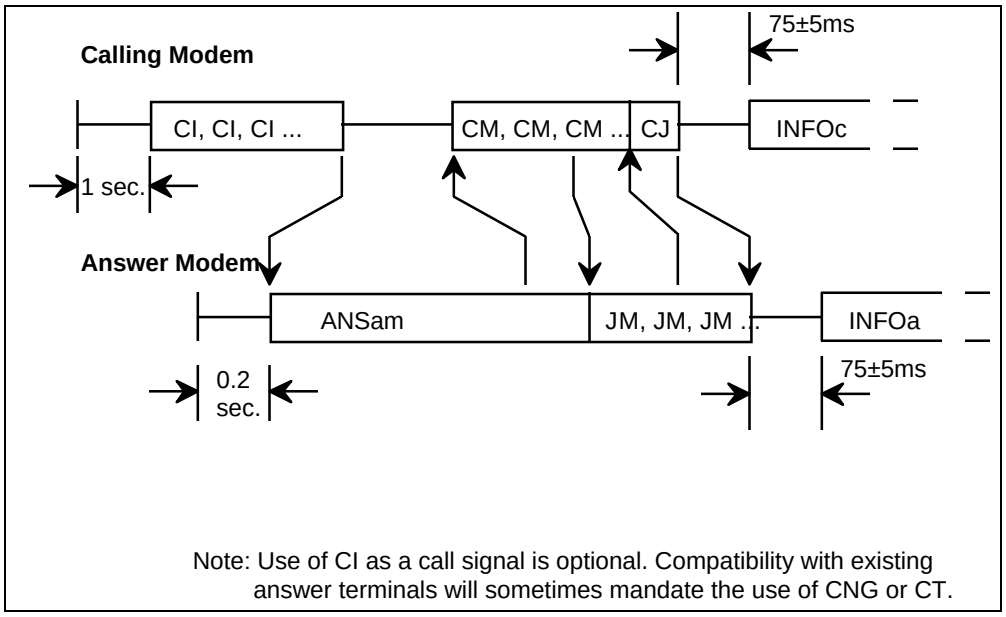


Figure 7-2. V.8 Procedures - Phase 1 Exchange

After 75 +/-5 ms of silence, Call Modem sends the INFOc sequence followed by Tone B (1200Hz) with phase reversals (/B). The Answer Modem sends INFOa sequence followed by Tone A (2400 Hz) with phase reversals (/A).

All INFO sequences are sent using DPSK at 600 bps with the split band.

The INFO sequence contains: supported symbol rates, carrier frequency capability, transmit power reduction capability, maximum difference in symbol rates between TX and RX paths, transmit clock source.

After detecting the Tone A phase reversal, the Call Modem continues to transmit Tone B for another 40 ms and then transmits a Tone B phase reversal for 10 ms.

Next, the Call Modem transmits L1and L2 line probing signals as defined in V.34. These signals are sets of probing tones with the repetition rate 150 Hz and spacing 150 Hz. At the end of this phase Answer Modem sends the INFOh sequence -- Frame Sync, minimum transmit power, length of TRN to be transmitted, carrier frequency, pre-emphasis filter requested, symbol rate, etc. The Phase 2 procedures are shown in Figure 7-3.

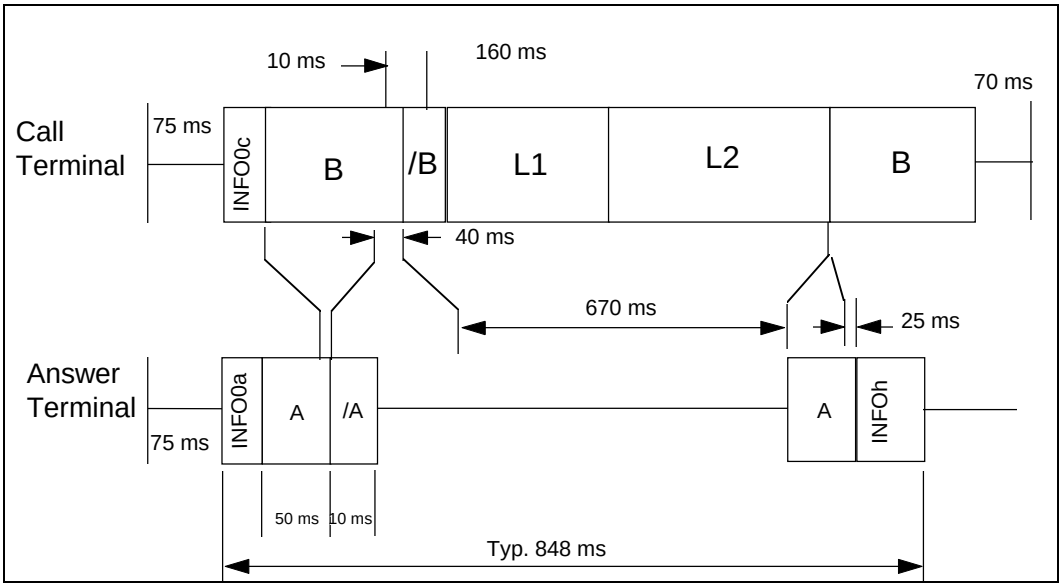


Figure 7-3. V.34 Line Probing (Phase 2)

Figure 7-4 shows Phase 3 V.34 HDX training. All signals are transmitted using the selected symbol rate, carrier frequency, pre-emphasis filter, and power level. This half-duplex training procedure is used to train the equalizer. All signals: S, /S, PP and TRN are defined in V.34 and are using the V.34 modulation. The constellation size and duration of TRN are set according to the INFOh sequence received from the recipient modem.

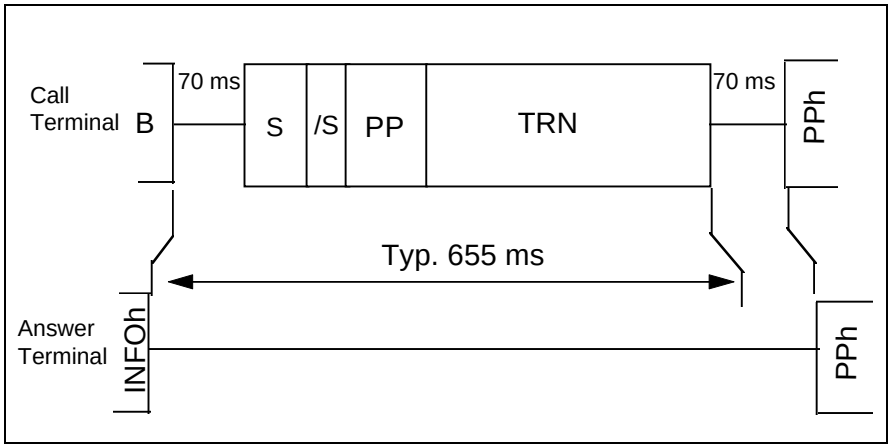


Figure 7-4. V34 HDX Training Procedure (Phase 3)

Phase 4 (Figure 7-5) is a control channel start-up and is used for final parameter exchange in the V.34 HDX handshaking. PPh is used in half-duplex mode for control channel receiver initialization and resynchronization. Modulation Parameter Sequences are exchanged between modems and contain modulation parameters to be used for the data transmission. The MPh symbols are transmitted using the control channel modulation at 1200 bps. At the end of this phase both modems send the E sequences to signal the beginning of control channel user data. It uses the control channel modulation at 1200 bps.

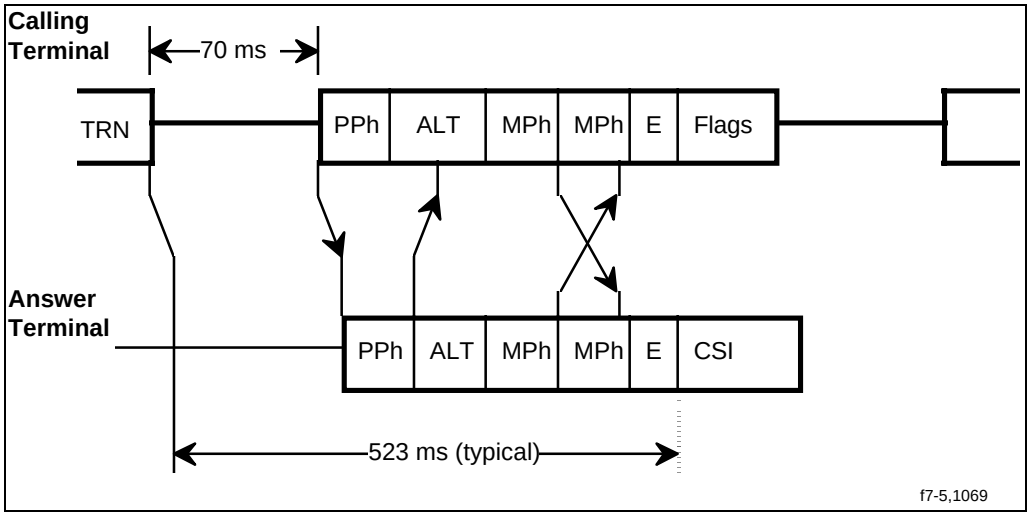


Figure 7-5. V34 Parameter Exchange

In Phase 5 both modems start the basic T.30 handshake (described in Chapter 6) using the control channel modulation at 1200 bps in a pseudo half-duplex fashion. The T.30 handshaking procedure is shown in Figure 7-6. (Phase 6 is the image data transmission phase.)

After the source modem transmits the image data using the primary channel (PC), it transmits the turn-off sequence followed by 70+/-5ms of silence. After this both modems go to control channel. Basically this exchange can be divided into two parts: Page confirmation using the control channel (and T.30 procedures), and V.34 HDX resync. The procedure between pages is shown in Figure 7-7.

The PC turn-off sequence (Figure 7-7) consists of a 35 ms transmission of "scrambled ones". At the end of the CC channel–after receiving CFR, MCF or other post message response–the source terminal will transmit consecutive "1"s until silence is detected from the recipienct terminal and at least 40 ones have been sent.

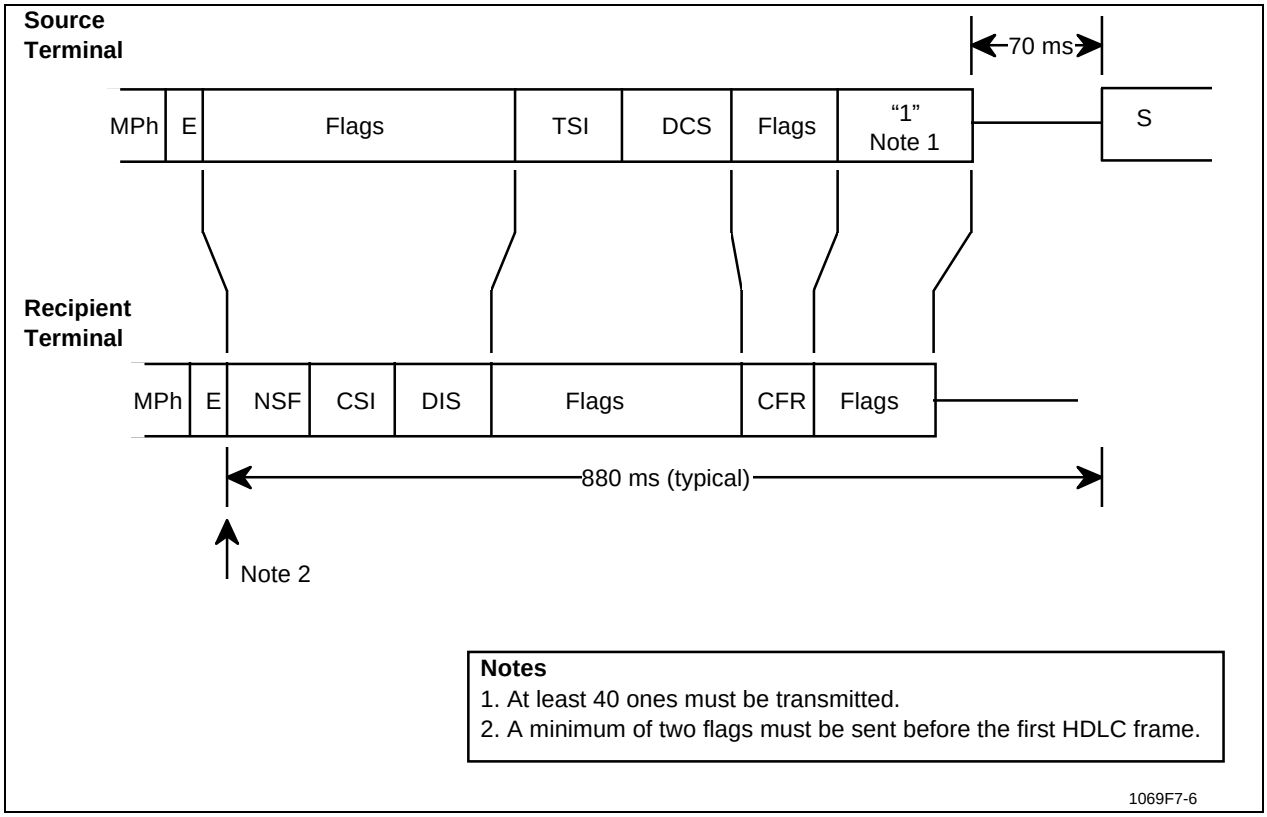


Figure 7-6. T.30 Fax Handshaking (Phase 5)

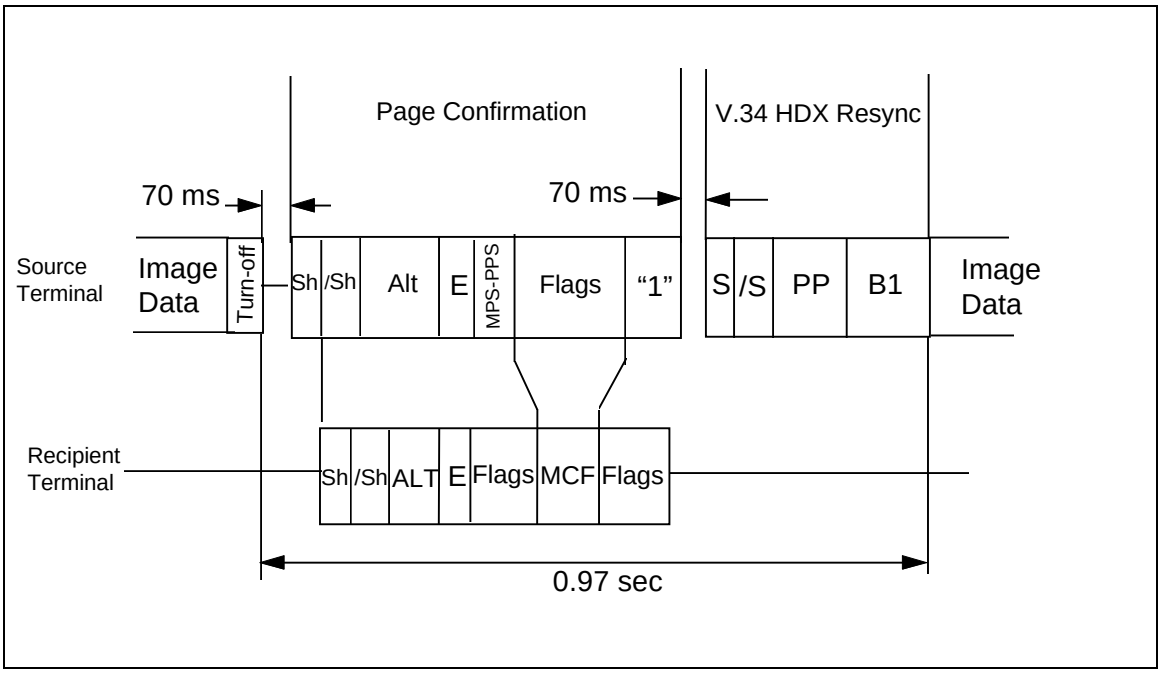


Figure 7-7. Inter-Page Procedure

7.2 Start-up Scenarios

All fax machines implementing V.34FAX ability must preserve the compatibility with existing traditional fax machines. To support existing fax machines, all fax start-up scenarios must be considered.

Four basic types of start-up scenarios (two automatic and two manual) are discribed below.

Automatic start scenarios

- Error free
- With errors

Manual start scenarios

- Error free
- With errors

There are three interoperability cases

- Call modem is V.8; Ans modem is V.8
- Call modem is V.8; Ans modem is V.21
- Call modem is V.21; Ans modem is V.8

Definitions:

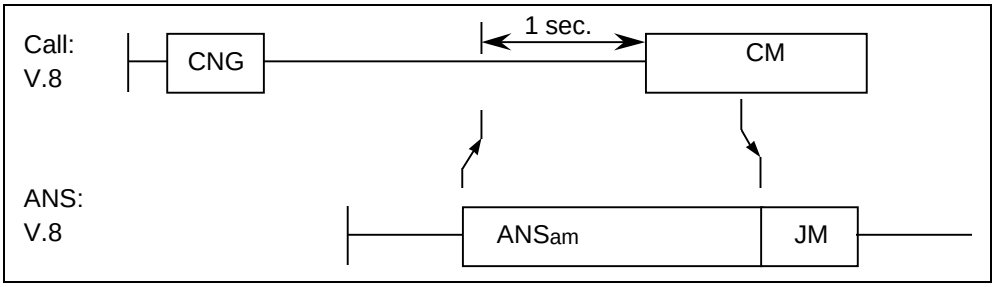
- V.8 terminal refers to a terminal with V.8 ability enabled. This includes transmitting ANSam when answering a call.
- V.21 terminal refers to a traditional T.30 terminal that does not have V.8 ability or does not have V.8 ability enabled.

7.2.1 Automatic Start Scenerios

Error-free Automatic Start

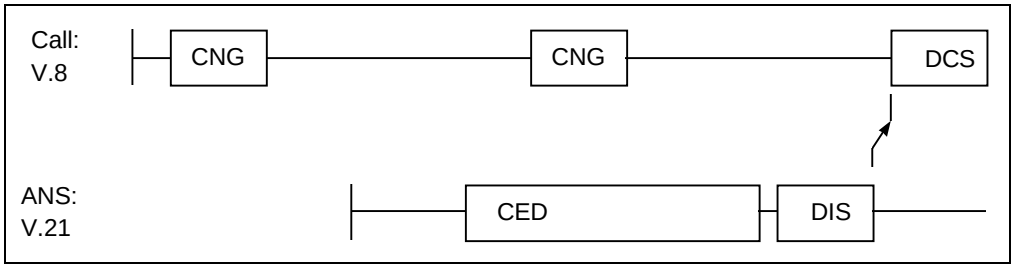
There are 3 primary cases for error-free v.8 startup when both terminals are configured in automatic mode:

Call: V.8, ANS: V.8

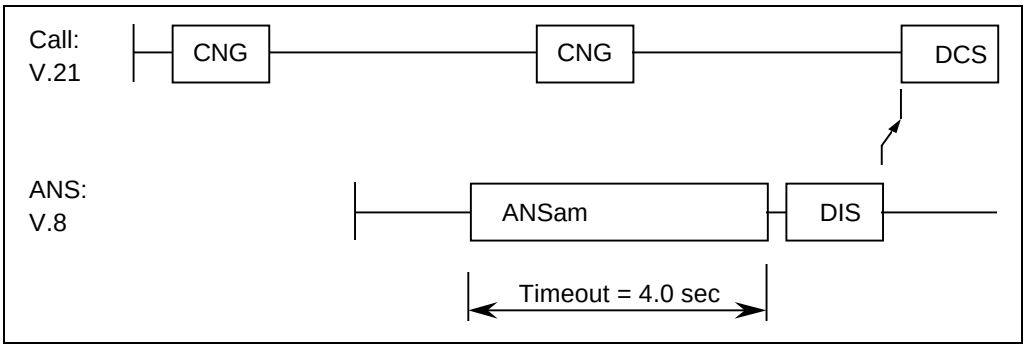


Note that the originate and answer modems (that is, direction of half duplex line probing) depends on the Call Function octet of V.8. The typical case is Call Function #4 (b5=0, b6=0, b7=1) where the line probing tones are sent from the call modem because the call modem is transmitting a fax to the answer modem. In the initial polling case (Call Function #5, b5=1, b6=0, b7=1), the line probing tones are sent from the **Answer** modem since the call modem wants to **receive** a FAX.

Call: V.8, ANS: V.21



Call: V.21, ANS: V.8



Automatic Start with Errors

Call: V.8, ANS: V.8

- If ANSam is completely missed, there is no recourse on the call side. Caller should try to detect DIS.
- If ANSam is interpreted as CED, the answer modem will still have DIS bit 6 set so a "manual type" V.8 startup call will still lead to a V.8 negotiation.
- If CM is missed, V.8 section 8.2.2/V.8 paragraph 4 indicates …continue as in T.30. Since CM was not received in response, the answer modem should send DIS and have bit 6 set even though it would appear that the other terminal is not V.8 capable since it did not respond to ANSam.
- If JM is missed or 2 identical JM sequences have not been received, no error recovery is defined in V.8 on the call side. The answer side continues to send JM (because it would not receive the JM terminating CJ) and can terminate using its own criteria (8.2.3/V8 paragraph 2) and then possibly transmit DIS. The call side must be prepared to detect JM and V.21H (DIS).

Call: V.8 -> ANS: V.21

- If CED is missed, no problem since CED is optional.
- If DIS is missed, DIS is repeated as per T.30.

Call: V.21 -> ANS: V.8

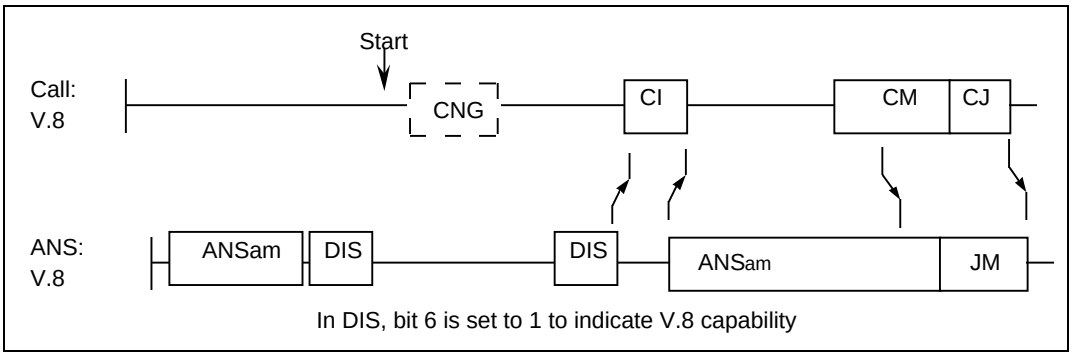
- If ANSam is missed, no problem since CED (as ANSam) is optional.
- If DIS is missed, DIS is repeated as per T.30.

7.2.2 Manual Start Scenerios

Error-free manual start

Manual Sending

Call V.8 -> ANS: V.8

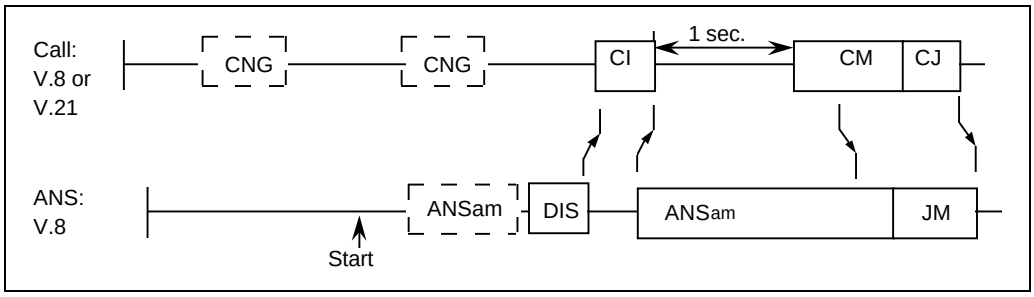


Call V.8 -> ANS: V.21

Call starts with optional CNG and is set to detect V.21. Since bit 6 will be set to 0, Call modem will proceed with original type negotiations using V.21.

Manual Receiving

Call: Unknown (V.8 or V.21) -> ANS: V.8



Call: Unknown (V.8 or V.21) -> ANS: V.21

Proceeding as in existing T.30

Manual Start with Errors

Call V.8 -> ANS: V.8

If CNG is missed or, optionally, not sent, DIS should continue to be transmitted as per the existing T.30 state.

If DIS is missed, DIS should automatically repeat if it does not receive any response.

If CI is missed, DIS should repeat.

The rest of the error cases are the same as the automatic scenarios.

Call V.8 -> ANS: V.21

Proceed as in existing T.30. (DIS repeats until response received.)

Manual Receive with Errors

Call: Unknown (V.8 or V.21) -> ANS: V.8

If DIS is missed, CNG will, optionally, continue to repeat. DIS will continue to repeat while waiting for a response.

If CI is missed, DIS will continue to repeat.

If ANSam is completely missed, there is no recourse on the call side. (Per section 7.2/V.8 paragraph 4, "A call DCE shall not transmit a signal CM unless ANSam has been detected."). Caller should try to detect DIS.

Call: Unknown (V.8 or V.21) -> ANS: V.21

Proceeding as in existing T.30

7.3 Turnaround Polling Scenerios

Turnaround polling involves changing the direction of fax transmission. Since the direction of the high data rate will be reversed, network providers need to be informed of this change through V.8 type means, so that they can reconfigure demod/remod equipment if necessary.

Traditional V.8 will not send CM until ANSam is detected (V.8 section 7.2/V.8) but in the turnaround polling cases, transmission of CM will commence the "V.8" exchange even though an ANSam signal will not be sent by the answer modem.

7.3.1 Changing from Transmit to Receive Fax

Figure F.5.11/T.30 illustrates the case of a call terminal transitioning from transmitting a fax to receiving a fax. Immediately after receiving forty "1"s from the recipient modem, the calling modem turns off the control channel by turning DTR off, waits 70 $\pm$5ms, and then initiates a V.8-like exchange by transmitting CM.

7.3.2 Changing from Receive to Transmit Fax

Figure F.5.12/T.30 illustrates the case of a call terminal transitioning from receiving a fax to transmitting a fax. As in the typical transition into the primary channel, the source (call) modem will transmit "1"'s and will wait for the recipient modem to turnoff. Then the source modem will turnoff its control channel, transmit silence for 70 +/- 5 ms and then transmit CM.

7.4 Summary of Signal Detectors at each phase

7.4.1 Call Terminal

During transmission of (optional) CNG, need to detect:

- ANSam (Auto, Error-free, V.8 -> V.8)
- CED (ANS) (Auto, Error-free, V.8 -> V.21)
- DIS (V.21(H)) (Manual, Error-free, V.8 -> V.8/V.21) since CED is optional in the manual receive case.

During transmission of CI, need to detect :

- ANSam (Manual, Error-free, V.8 -> V.8)
- DIS (V.21(H)) (Error, V.8 -> probable V.8)

During transmission of CM need to detect :

- ANSam (Manual, Error-free, V.8 -> V.8)
- JM (Error-free, V.8 -> V.8)
- DIS (V.21(H)) (Error: answer missed CM)

7.4.2 Answer Terminal

During transmission of ANSam, need to be able to detect:

- CM (Auto, Error-free, V.8 -> V.8)
- CNG (Auto, Error-free, V.21 -> V.8)

During transmission of DIS (with bit 6 set) must be able to detect and receive:

- CI (V.21(L)) (Manual, Error-free, V.8 -> V.8)
- DCS (V.21(H)) (Manual, Error-free, V.21 -> V.8)

During turnaround polling, need to be able to detect:

- CM (Auto, Error-free,)

7.5 OPERATION

The host can access several registers in RAM to control and monitor V.8 operation (see Section 4). There are five control registers (Table 7-1) and three status registers (Table 7-2). The host also has access to registers that contain the configuration (CONF) codes associated with the modulation modes of operation (Table 7-3).

To enter V.8 mode, load the interface memory CONF register with AA and then set the NEWC bit. Negotiation begins when DTR is set by the host.

7.5.1 ORIGINATING MODEM OPERATING PROCEDURE

Originating modem negotiation procedures may be started by sending CNG or CI.

(CI will be sent if the host sets register 304 bit 2 while in V.8 mode)

Originating with CNG

The basic automatic-to-automatic origination procedure is shown in Figure 7-8. Some of the configuration details are shown in Figure 7-9.

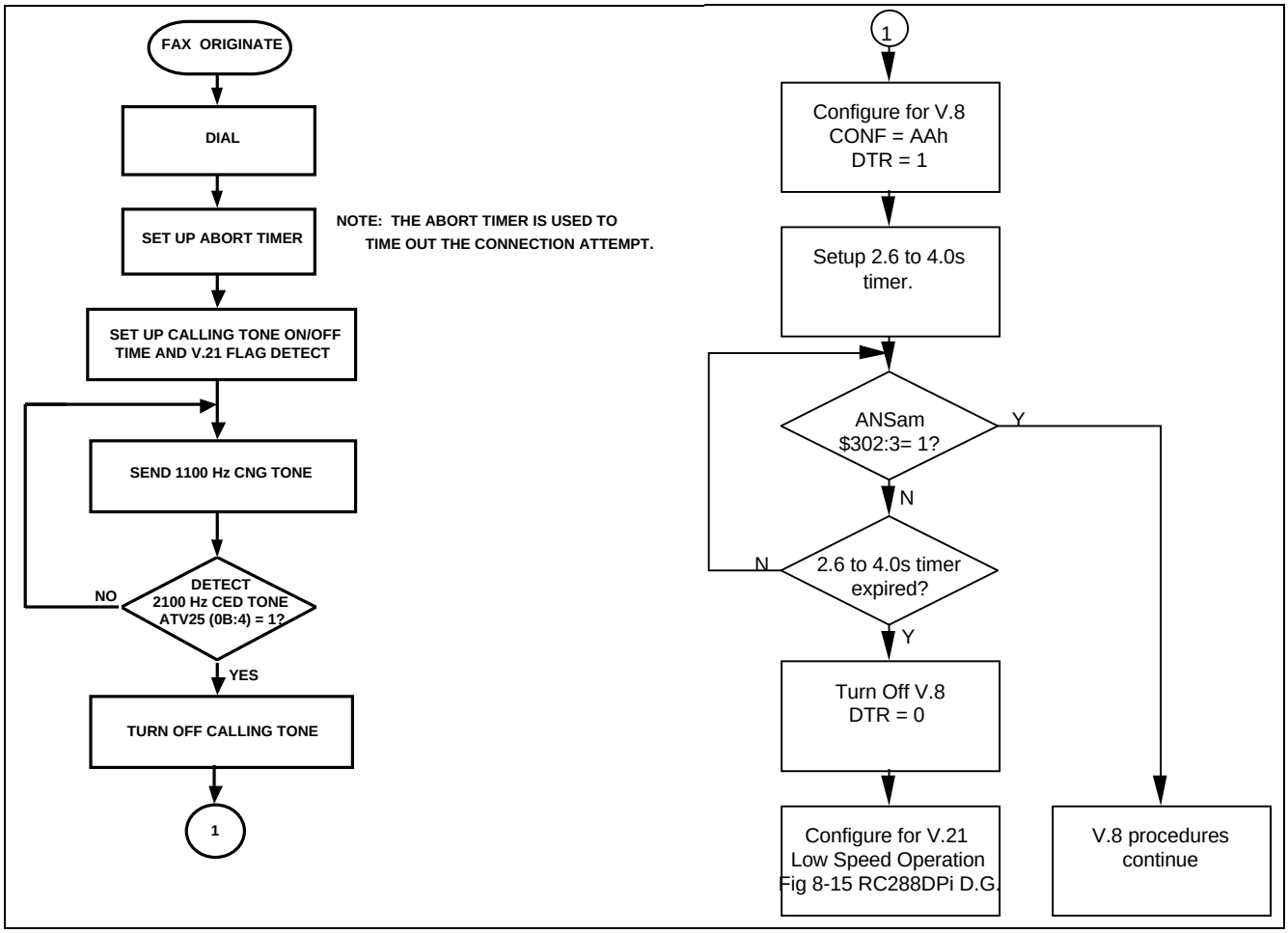


Figure 7-8. Automatic to Automatic Origination and Operation

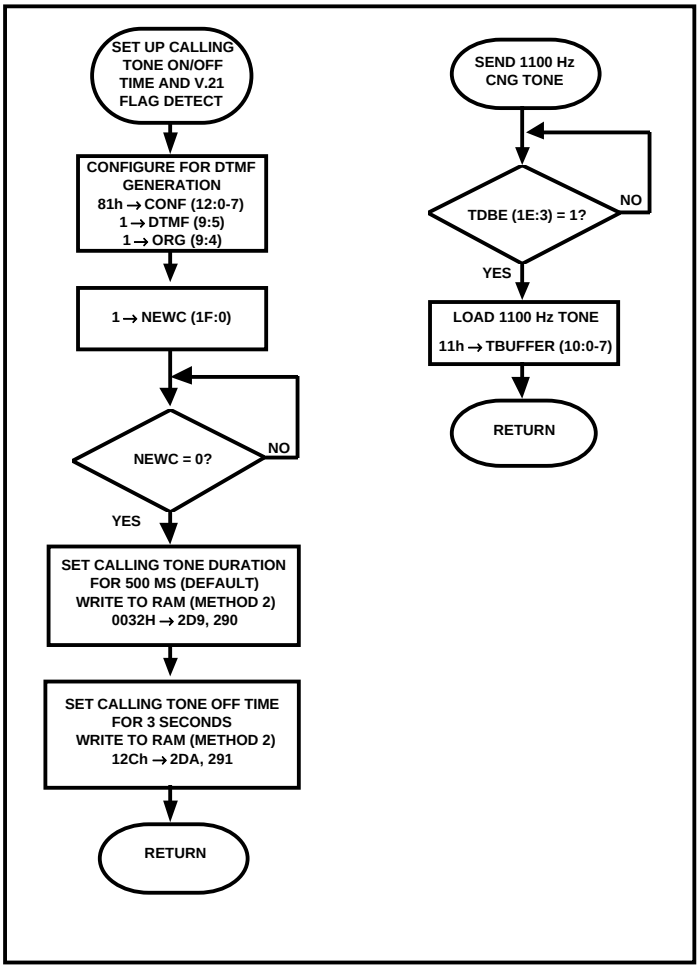


Figure 7-9. Configuration Procedures

After dialing, Figure 7-8 shows monitoring bit ATV25 (0B:4) to detect ANS (CED) or ANSam and FLAGDT (0A:6) to detect V.21 Flags. If ATV25 is set, to discriminate between CED and ANSam, configure and initiate V.8 by setting CONF = AA, set NEWC, and then set DTR.

In (V.8) originate mode, the transmitter is set up to transmit Silence by default ($38F:3 = 0 and $304:2 = 0). The receiver is set up to detect ANS and ANSam. The data pump sets register 301 bit 5 when ANS is detected and register 302 bit 3 if ANSam is detected. In the case of ANSam signal, the ANS bit will be set before the ANSam bit. The bit turn on timing depends on the line conditions and receive levels.

If ANS only (i.e., CED) is detected, V.8 mode is stopped by turning DTR off and then prepare to receive V.21 signals by setting CONF = A8 and proceed as described in chapter 6.

Once ANSam is detected, the transmitter waits a silence period before transmitting CM. The silence period is 500 ms if no phase reversals are detected in ANSam, otherwise the silence period is 1 second. The CM sequence consists of a Preamble, followed by a SYNC octet, a Data Call Function Category octet, at least one modulation mode octet, an optional protocol octet, and an optional GSTN octet (Table 7-4). The 16-byte transmit buffer, located at address 32D, is loaded with the CM sequence once ANSam is detected.

The number of modulation mode octets transmitted is a function of the bit settings in control registers 306 to 308 (Table 7-1). For example, if no modulation bits are set in registers 307 or 308, then only one modulation octet is sent (modn0). On the other hand, if bits are set in register 307, but not in register 308, then modn0 and modn1 are sent. Only when register 308 contains non-zero modulation bits will all three modulation octets be sent.

The protocol octet is transmitted if register 305 bit 0 is set. The 3-bit protocol field is located in register 305 bits 5-7. The default protocol bits are set to indicate LAPM availability. The GSTN octet is sent if address 304 bit 4 is set. The GSTN octet will be sent indicating cellular access if address 305 bit 2 is set.

CM transmission continues until JM is detected. When JM is detected, the current CM octet is completed and then CJ is appended to the transmitted data stream. A 75 ms silence period follows CJ transmission and the CONF register is updated

to the "Modulation Mode" indexed by the highest common modulation mode in JM (Table 7-3). If no modulation modes are common, the CONF register changes to C0h, the "V.8 Cleardown" mode.

Originating with CI

In some cases of delayed or manual start, an originating modem may not receive an ANSam signal but it does receive a V.21 DIS frame with bit 6 (V.8 capability) set to 1. The call modem should then prepare to send CI by setting CONF = AAh and $304:2 to 1.

Once DTR transitions on, the transmitter is silent for 400 ms before the CI sequence (Table 7-5) is transmitted. CI is sent with a regular cadence of 1 second on and 1 second off. The on and off times are accessible via memory access. In particular, the on time counter, MaxFrameByteCount, is located at $31C. This counter is a "byte" counter and defaults to 30 bytes for CI transmission. (Note that the MaxFrameByteCount should not be less than 9 {= 3 frames} if the minimum three frames of CI is desired.) If this location is negative (i.e., MSB = 1), then there is no cadence applied to the transmitted V.8 frame.

Note: MaxFrameByteCount = FFh when transmitting CM and JM.

The CI cadence will continue until ANSam is detected and the minimum three CI frames have been transmitted. Upon detection of ANSam, CM is sent in the manner described earlier in this paragraph.

7.5.2 Answering Modem Operating Procedure

General Procedures and Automatic Start

After the host goes off-hook, it configures the modem to send a V.8 ANSam answer tone. The caller may be another V.8 machine or an original V.21 only terminal, one of the following 2 paths (following paragraph or 7.5.2.2) will need to be followed depending on the calling modem's response to ANSam.

When configured as the V.8 answer modem, the modem will transmit ANSam if $38F:3 =0 and $304:1 = 0. The host can monitor when the modem begins transmitting ANSam by observing $300:0; when set the modem has begun transmitting ANSam. The modem does not reset $300:0 when transmission of ANSam is completed. The host should initiate a 2.6 to 4.0 second timer when the modem begins transmitting ANSam, if the originate modem does not respond to ANSam with CM, the host should reconfigure for V.21 transmission (see below). The receiver will detect V.8 frames CI, CM, and CJ. Register 301 bits 1-3 hold the status of CM, CI, and CJ detection (see Table 7-2). If CM was detected, continue with section 7.5.2.3.

V.21 only, Manual V.8, or Late Start

If no V.8 frames are detected, and the 2.6 to 4.0 second timer has expired, the host should prepare the modem to transmit V.21 and send a DIS frame with bit 6 set to indicate V.8 capability. The host shall turn off DTR, set CONF = A8, set NEWC, set RTS after 75±5ms, and transmit (NSF)DIS frames as described in Chapter 6. Immediately after the DIS frame is transmitted, the host shall reconfigure the modem in V.8 and set $304:1 to have the modem not transmit ANSam until after CI is received. The host should also program one of the Supervisory Tone Detectors to detect V.21 flags from a possible DCS frame coming from the call modem.

If V.21(H) flags are detected, the modem should be configured for V.21(H) operation (CONF=A8) and the original T.30 procedures described in Chapter 6 shall be followed. If CI is detected, the modem will send ANSam and proceed with a V.8 negotiation as described in paragraph 7.5.2.3.

V.21(H) Flag Detection during V.8

This subsection describes how to configure any of the three Supervisory tone detectors to detect V.21 High Channel HDLC Flags. This detector complements the FLAGDT bit, which does not run in V.8 modes. This is due to the architecture of the V.8 receiver. However by implementing this tone detector, a host can detect the appearance of FLAGS in V.8 modes.

Using the same naming convention as is defined in function 27-29, the tone detector coefficients are

	BIQUAD #1	BIQUAD #2
A3	$0666	$0666
A2	$FFDD	$1C04
A1	$0666	$0666
B2	$0F71	$FEA2
B1	$C146	$C289
THRESHU		$2000
THRESHL		$2000

The threshold values will require tuning to the hosts particular requirements, but a suggested value of 2000hex in both Upper and Lower Thresholds (i.e. No Hysteresis) is a reasonable starting point.

V.21(L) Flag Detection during V.21(H)

This paragraph describes how to configure any of the three Supervisory tone detectors to detect V.21 Low Channel. (Bandpass filter 980-1180Hz, stopband better than -40dB, sample rate 7200Hz)

Using the same naming convention as is defined in function 27-29, the tone detector coefficients are

	BIQUAD #1	BIQUAD #2
A3	$0D11	$0D11
A2	$E5F7	$0D11
A1	$0D11	$0D11
B2	$CC29	$CE1A
B1	$5175	$3430
THRESHU		$0010
THRESHL		$0001

After V.8 is started (CM detected)

When CM is detected, a JM frame is constructed using parameters from CM (Table 7-6). The JM sequence starts with the 10 ONES preamble followed by the synchronization octet. Next comes the call function. If the received CM octet contains the same call function as the answer modem's "preferred" call function (register 304 bits 5-7), then the same call function that was received in CM is also sent in JM.

If the CM octet contains a different call function that the "preferred" call function, then the CallFunctionAllowed register (address 32A) is consulted (see Table 7-7). The host can set up the CallFunctionAllowed register to indicate the call functions that it allows. It is a bit-mapped register where an appropriate bit is set if corresponding call function is to be allowed. If the call function received in CM does not match any allowable call functions, then the preferred call function is returned with all modulation bits set to zero. On the other hand, if the call function is allowed, the answer modem will respond with the same call function as that received in CM.

JM will contain all the necessary modulation octets needed to reflect the jointly common modulation modes available at the answer modem and received in the CM sequence. If, however, address 305 bit 1 is set, then JM will contain the minimum number of modulation octets needed to convey the highest common mode. If no modulation modes are common, then the JM frame will send all modulation octets with none of the modulation bits set.

The protocol octet is sent only if the received CM contained a protocol octet AND control register 305 bit 0 is set. The GSTN octet is sent if control register 304 bit 4 is set OR if the received CM contained a GSTN octet. The GSTN octet will be sent indicating cellular access if control register 305 bit 2 is set.

If V.34 Half Duplex is negotiated, the modem will automatically continue with the V.34 startup procedures. The handshaking can be monitored using the information in paragraph 7.6

If V.17, V.29, or V.27 are negotiated, the host shall turnoff DTR (ending V.8) and proceed with configuring the modem for V.21 channel 2 (low speed) operation as discussed in Chapter 6.

Table 7-1. V.8 Host Control Bits

Address (Hex)	7	6	5	4	3	2	1	0	Default Value (Hex)[1]
304	Call Function to be Transmitted			Send GSTN Octet	No PN+ID with ANSam	Transmit CI	No TX of ANSam until CI Detected	VFC Over V.8	88
305	Protocol Bits to be Transmitted			X	**No RLSD in V.8**	Cellular Access	Send Minimum JM Sequence	Send Protocol Octet	08
306	V.34 HDX	**V.34 FDX**	X	X	X	X	X	X	80
307	V.27	V.29	X	X	X	V.17	X	X	C4
308	**V.21**	V.23 HDX	X	X	X	**V.23 FDX**	X	X	80
38F	X	X	X	X	CM without ANSam	X	X	X	----0---

Notes: 1. Default values are written at POR. 2. Default bits turned on are indicated in bold.

Table 7-2. V.8 Status Bits

Address (Hex)	7	6	5	4	3	2	1	0	Default Value (Hex)*
300								Sending ANSam	00
301	VFC ID found	FSK Byte Ready	ANS Detected	JM Detected	CJ Detected	CM Detected	CI Detected	Min CI Sent	00
302	Received Call Function			Protocol Octet Received	ANSam Detected			No Modes Common	00
303	Received Protocol Bits						Remote is using Cellular	Received GSTN Octet	00

* Cleared on NEWC with CONF = AAh.

Table 7-3. Modulation Modes

Address (Hex)	Configuration	Default Value (Hex)[1]
30A	V.34 half duplex - 28.8kbps	CC
30D	V.17 (Note 3)	A8
30E	V.29 (Note 3)	A8
30F	V.27 (Note 3)	A8
312	V.23 full-duplex (Note 2)	A4
313	V.23 half-duplex	A4
314	V.21 Channel 2	A8

Notes:

1. See CONF codes in Table 3-1.
2. Default value assumes V.23 answer mode; change to A1 for V.23 originate mode (see CONF bits in Table 3-1).
3. The default configuration of the modes is A8 (V.21 channel 2) so that the modem will automatically configure the modem for V.21 channel operation immediately after V.8. The answer terminal host must set RTS 70 $\pm$ 5 ms after V.8 is complete.

Table 7-4. CM Frame

Address (Hex)	Octet	Default Value (Hex)
	Preamble	FF
32D	SYNC CM	E0
32E	Data Call Function	C1
32F	modulation 0	40
330	modulation 1 *	13
331	modulation 2 *	94
332	Protocol (optional)	1A
333	GSTN (optional)	2D
334	Frame End	7E
* if necessary		

Table 7-5. CI Frame

Address (Hex)	Octet	Default Value (Hex)
	Preamble	FF
32D	SYNC CI	00
32E	Data Call Function	C1
32F	EOF	7E

Table 7-6. JM Frame

Address (Hex)	Octet
	Preamble
32D	SYNC JM
32E	Call Function from CM
32F	Common modulation 0
330	Common modulation 1 *
331	Common modulation 2 *
332	Protocol (optional)
333	GSTN (optional)
334	Frame End
* if necessary	

Table 7-7. Call Functions Allowed

Address (Hex)	7	6	5	4	3	2	1	0	Default Value (Hex)
32A	CF 7 Allowed (extension)	**CF 6 Allowed (Duplex data)** b7=1 b6=1 b5=0 oct=$C1	CF 5 Allowed (FAX-RX) b7=1 b6=0 b5=1 oct=$A1	CF 4 Allowed (FAX-TX) b7=1 b6=0 b5=0 oct=$81	CF 3 Allowed	CF 2 Allowed (V.18)	CF 1 Allowed	CF 0 Allowed	$40

7.5.3 OPERATION during TURNAROUND POLLING.

Following description refers to Figure F.5.11/T.30

TX to RX

Call Terminal

Once the modem has detected at least forty "1"'s, the modem will set bit PNSUC. The host should read any remaining data in RBUFFER, reset bit PNSUC, and turnoff DTR. The host should set CONF=AA, set NEWC, and set the "CM without ANSam" bit ($38F:3) to 1. The host must set DTR within 70 +/- 5m after DTR was reset.

Answer Terminal

After the host has successfully received the T.30 DTC signal, the host should set MHLD (07:0) to indicate that the modem should begin transmitting consecutive "1"s. When RLSD has turned off, the host should set CONF=AA, set NEWC, set the "CM without ANSam" bit ($38F:3) to 1 and set DTR.

RX to TX

Call Terminal

After the host has successfully received the T.30 DTC signal, the host should set RTS to indicate that the modem should begin transmitting consecutive "1"s. When RLSD has turned off, the host should set CONF=AA, set NEWC, and set the "CM without ANSam" bit ($38F:3) to 1 . The host must set DTR within 70 +/- 5ms after RLSD was turned off.

Answer Terminal

When RLSD has turned off, the host should set CONF=AA, set NEWC, set the "CM without ANSam" bit ($38F:3) to 1 and set DTR.

7.5.4 OPERATION during INITIAL POLLING.

Call Terminal

If the calling terminal wishes to allow standard transmit and initial polling, it must set the Call Function Allowed register $32A to $30 and set register $304 according to the preferred first function. If only initial polling is desired, set $32A = $20 and $304 = A8.

Monitor the CM/JM exchange. If JM indicates RX-FAX, during the silence period, reset the ORG bit.

Answer Terminal

If the answer terminal wishes to do an initial polling as it's first call function, it should set $32A = $20 and $304 = A8. Monitor the CM/JM exchange. If JM indicates RX-FAX, during the silence period, set the ORG bit.

7.6 HANDSHAKE MONITORING

7.6.1 Octet Monitoring

During the V.8 (Phase 1) procedure the received V.8 octets can be read from the interface memory RBUFFER register by clearing bit $305:3 of the V.8 host control bits. The procedure is the same as accessing receive data during normal data mode.

7.6.2 V.34 Handshake Phase Monitoring

During the V.8/V.34 handshake, the secondary channel data buffers display the "state" of the receiver (SECRXB) and the transmitter (SECTXB). Bits 5, 6 and 7 of these buffers indicate the phase of the handshake (see Table 7-8 and Table 7-10).

Using the New Status (NEWS) function, an interrupt can be generated whenever a change occurs to SECRXB and SECTXB. The NEWS masks for these locations are $370 and $371, respectively. For a full description, refer to Chapter 4.

Table 7-8. Receiver Handshake Phase and States

Register (Hex)	7	6	5	4	3	2	1	0
16 SECRXB	Receiver Handshake Phase (See box below.)			Receiver Handshake State				

Bits 5-7: Receiver Handshake Phase.

Bit 7	Bit 6	Bit 5	SECRXB Value	Handshake Phase (ITU Specification)
0	0	0	0x	Phase 1 (V.8)
0	0	1	2x	Phase 2 (V.34)
0	1	0	4x	Phase 3 (V.34)
1	0	0	8x	Phase 4 (V.34), Phase 5 (T.30 handshaking)
1	0	1	Ax	Phase 6 (V.34)

Bits 0 -4: Receiver Handshake Phase States.

Phase 1

See Table 7-9.

Table 7-9. Receiver Handshake Phase 1 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Originate Mode Receiver State	Answer Mode Receiver State
0	0	0	0	0	00	Looking for ANSam	Looking for CI or CM
0	0	0	0	1	01	Found ANSam, looking for JM	Found CI, looking for CM
0	0	0	1	0	02	Found JM	Found CM, looking for CJ
0	0	0	1	1	03	NA	CJ detected

Phase 2

See Figure 7-8.

Phase 3

See Figure 7-8.

Phase 4

See Figure 7-8.

Table 7-10. Transmitter Handshake Phase and States

Register (Hex)	7	6	5	4	3	2	1	0
17 (SECTXB	Transmitter Handshake Phase (See box below.)			Transmitter Handshake Phase State				

Bits 5-7: Transmitter Handshake Phase

Bit 7	Bit 6	Bit 5	SECTXB Value	Handshake Phase (ITU Specification)
0	0	0	0	Phase 1 (V.8)
0	0	1	1	Phase 2 (V.34)
0	1	0	2	Phase 3 (V.34)
1	0	0	8x	Phase 4 (V.34), Phase 5 (T.30 handshaking)
1	0	1	Ax	Phase 6 (V.34)

Bits 0 -4: Transmitter Handshake Phase State.

Phase 1

See Table 7-11 and Table 7-12.

Table 7-11. Transmitter Handshake Phase 1 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Call Modem Transmitter State SECTXB	Answer Modem Transmitter State SECTXB
0	0	0	0	0	00	Pausing 400 ms (Transmitting silence)	Sending ANSam
0	0	0	0	1	01	Sending CI	Sending JM
0	0	0	1	0	02	Sending Silence (500 ms or 1000 ms)	Sending Silence (75 ms)
0	0	0	1	1	03	Sending CM	NA
0	0	1	0	0	04	Sending CJ	NA
0	0	1	0	1	05	Sending Silence (75 ms)	NA

Table 7-12. Receiver Handshake Phase 1 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Call Modem Receiver State SECRXB	Answer Modem Receiver State SECRXB
0	0	0	0	0	00	Looking for ANSam	Looking for CI or CM
0	0	0	0	1	01	Found ANSam, looking for JM	Found CI, looking for CM
0	0	0	1	0	02	Found JM	Found CM, looking for CJ
0	0	0	1	1	03	NA	CJ detected

Phase 2

See Table 7-13 and Table 7-14.

Table 7-13. Transmitter Handshake Phase 2 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Transmitting Modem Transmitter State SECTXB	Receiving Modem Transmitter State SECTXB
0	0	0	0	0	00	Sending INFO0c	Sending INFO0a
0	0	0	0	1	01	Sending Tone B	Sending Tone A
0	0	0	1	0	02	Sending Tone /B	Sending Tone /A
0	0	1	0	0	04	Sending L1	NA
0	0	1	0	1	05	Sending L2	NA
0	0	1	1	0	06	Sending Tone B	NA
0	1	0	0	0	08	NA	Sending silence
0	1	0	1	0	0A	NA	Sending Tone A
0	1	1	0	0	0C	NA	Sending INFO0h

Table 7-14. Receiver Handshake Phase 2 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Transmitting Modem Receiver State SECRXB	Receiving Modem Receiver State SECRXB
0	0	0	0	0	00	Found silence, looking for INFO0a	Found silence, looking for INFO0c
0	0	0	1	0	02	Found INFO0a, looking for Tone A	NA
0	0	0	1	1	03	Found Tone A, looking for Tone /A	NA
0	0	1	0	0	04	Found Tone /A, looking for silence	NA
0	0	1	0	1	05	Found silence, looking for Tone A	NA
0	0	1	1	0	06	NA	Found INFO0c, looking for Tone B
0	0	1	1	1	07	NA	Found Tone B, looking for Tone /B
0	1	0	0	0	08	NA	Receiving L1
0	1	0	0	1	09	NA	Receiving L2
0	1	0	1	0	0A	NA	Received L2, looking for Tone B
0	1	1	0	0	0C	Found Tone A, looking for INFO0h	NA
0	1	1	1	0	0E	NA	Receiving Tone B

Phase 3

See Table 7-15 and Table 7-16.

Table 7-15. Transmitter Handshake Phase 3 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Transmitting Modem Transmitter State SECTXB	Receiving Modem Transmitter State SECTXB
0	0	0	0	0	00	Transmitting silence 70 ms	Transmitting silence
0	0	1	0	0	04	Sending S	NA
0	0	1	0	1	05	Sending /S	NA
0	0	1	1	0	06	Sending PP	NA
0	1	1	0	0	07	Sending TRN	NA

Table 7-16. Receiver Handshake Phase 3 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Transmitting Modem Receiver State SECRXB	Receiving Modem ReceiverState SECRXB
0	0	0	0	0	00	Receiving silence	Found silence, looking for S
0	0	0	0	1	01	NA	Found S, looking for /S
0	0	1	1	0	06	NA	Receiving PP
0	0	1	1	1	07	NA	Receiving TRN

Phase 4 and Phase 5 T.30 Handshaking

See Table 7-17 and Table 7-18.

Table 7-17. Transmitter Handshake Phase 4 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Transmitting Modem Transmitter State SECTXB	Receiving Modem Transmitter State SECTXB
0	0	0	0	0	00	Transmitting silence 70 ms	Transmitting silence 70 ms
0	1	0	0	0	08	Sending PPh	Sending PPh
0	0	0	0	1	01	Sending ALT	Sending ALT
0	0	0	1	0	02	Sending MPh	Sending MPh
0	0	0	1	1	03	Sending E	Sending E
0	0	1	0	0	04	T.30 Fax handshaking	T.30 Fax handshaking

Table 7-18. Receiver Handshake Phase 4 States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Originate Mode Receiver State SECRXB	Answer Mode Receiver State SECRXB
0	0	0	0	0	00	Receiving silence	Receiving silence
0	0	0	0	1	01	Receiving PPh	Receiving PPh
0	0	0	1	0	02	Received ALT, receiving MPh	Received ALT, receiving MPh
0	0	0	1	1	03	Received Mph, receiving E	Received Mph, receiving E
0	0	1	0	0	04	Receiving Flags and T.30 handshaking	Receiving Flags and T.30 handshaking

Phase 6 Primary Channel Resync and Image Data TX/RX

See Table 7-19 znd Table 7-20.

Table 7-19. Transmitter Primary Channel Resync and Image Data TX/RX States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Transmitting Modem Transmitter State SECTXB	Receiving Modem Transmitter State SECTXB
0	0	0	0	0	00	Transmitting silence 70 ms	Transmitting silence
0	0	1	0	0	04	Sending S	NA
0	0	1	0	1	05	Sending /S	NA
0	0	1	1	0	06	Sending PP	NA
0	0	1	1	1	07	Sending B1 and Image Data	NA
0	0	0	0	0	00	Transmitting Turn-Off sequence	NA

Table 7-20. Receiver Primary Channel Resync and Image Data TX/RX States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Transmitting Modem Receiver State SECRXB	Receiving Modem Receiver State SECRXB
0	0	0	0	0	00	Receiving silence	Receiving silence
0	0	0	0	1	01	NA	Receiving S and /S
0	0	0	1	0	02	NA	Receiving PP
0	0	0	1	1	03	NA	Receiving B1 and Image Data

Between Pages - No Data Rate Changes.

The phase number is 4, which corresponds to $8x values in SECRXB and SECTXB, where x is a State number, see Table 7-21 and Table 7-22.

Table 7-21. Transmitter States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Transmitting Modem Transmitter State SECTXB	Receiving Modem Transmitter State SECTXB
0	0	0	0	0	00	Transmitting silence 70 ms	Transmitting silence 70 ms
0	1	0	0	1	09	Sending Sh - /Sh	Sending Sh - /Sh
0	0	0	0	1	01	Sending ALT	Sending ALT
0	0	0	1	1	03	Sending E	Sending E
0	0	1	0	0	04	Sending Flags and MPS-PPS	Sending Flags and MCF

Table 7-22. Receiver States

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	State Number	Originate Mode Receiver State SECRXB	Answer Mode Receiver State SECRXB
0	0	0	0	0	00	Receiving silence	Receiving silence
0	1	0	0	1	09	Receiving Sh - /Sh	Receiving Sh - /Sh
0	0	0	1	0	02	Received Sh - /Sh, receiving ALT & E	Received Sh - /Sh, receiving ALT & E
0	0	1	0	0	04	Receiving Flags and MCF	Receiving Flags and MPS-PPS

7.6.3 Control Channel Retrain

To initiate a CC retrain, the initiating host shall set bit CCRTN. The modem will turn off the CTS and transmit the AC signal. The modem's receiver will be able to detect PPh. Figure 7-10 shows the retrain sequence of actions at the initiating and responding modems.

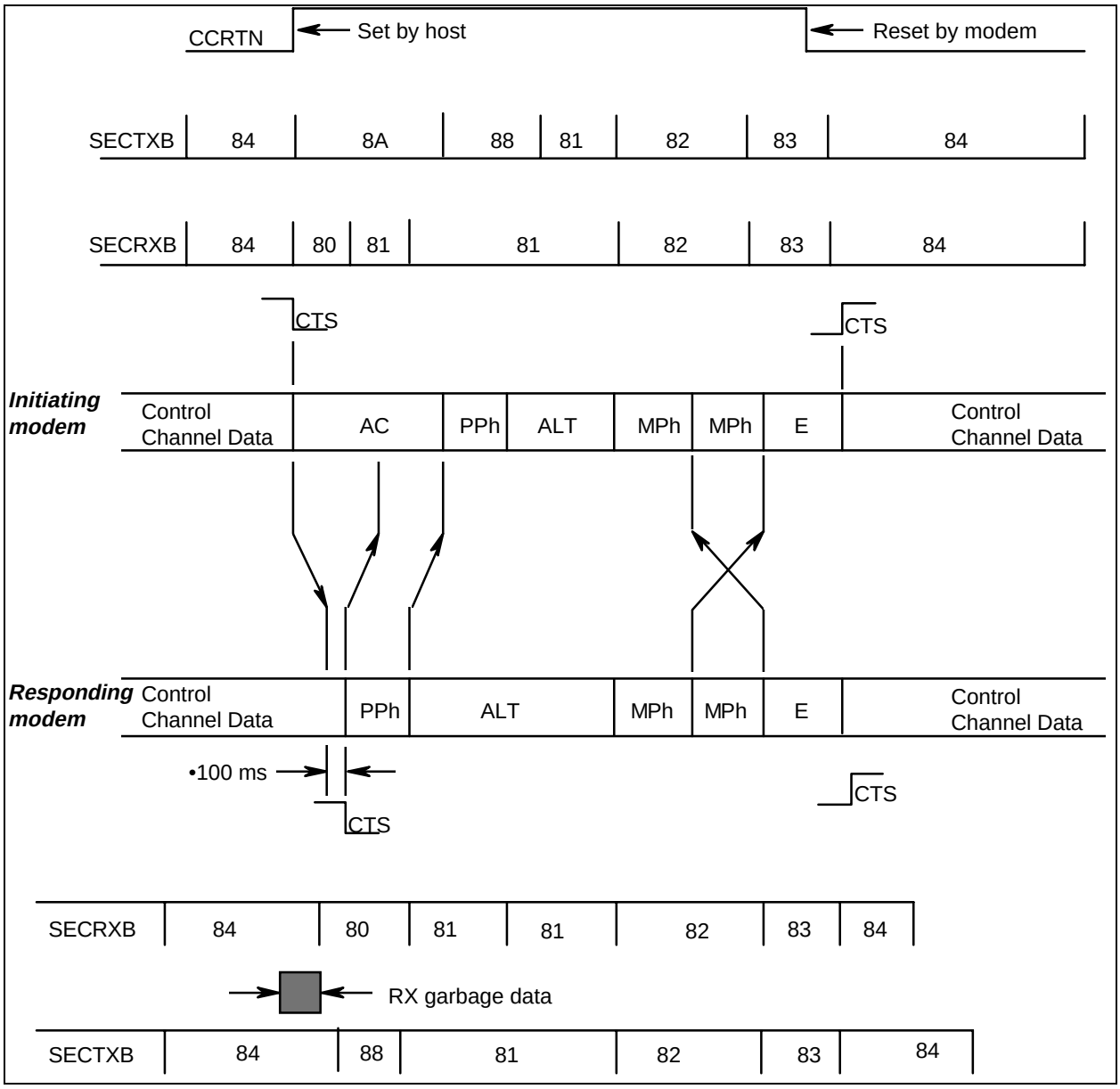


Figure 7-10. Control Channel Retrain Timing

There are two very important timing uncertainties to consider for V.34 training/resync/retrain procedures and timing diagrams as shown above:

1. A path's Trip Delay (one way) and Round Trip Delay play a very important part in the duration of, and relationship among, the signals shown. Since every connection will have a different delay time (for example, 30ms on a local call, 300 ms on a satellite) signals like MPh, which are repeatedly transmitted until 2 identical MPh frames are received, will significantly vary the number of MPh frames that are transmitted.
2. The length of a signal can vary according to manufacturers and implementation. For example, the duration of ALT can be anywhere from 16T to 120T. Thus a given timing diagram might not be to scale.

SECRXB and SECTXB are mainly for information for the host. The host should not take timing information from those registers. Host control implementation strategies may be based on the following:

- CC Initiating modem: After setting CCRTN, set a timer (about 1-2 seconds) to check for the end of CC retrain. (CTS turning on indicates CC retrain complete.)
- CC responding modem: During the control channel, the host should monitor SECRXB and SECTXB, if it ever changes from $84, then a CC retrain procedure is likely in progress. A timer should be set to make sure CTS is on again after 1-2 seconds.

The host can look at each and every state change, but there is not so much benefit in normal situations. If a procedure fails, it is helpful to take note of the SECRXB, SECTXB, and ABCODE values to diagnose the problem.

8. DESIGN CONSIDERATIONS

Good engineering practices must be adhered to when designing a printed circuit board (PCB) containing the modem device set. Suppression of noise is essential to the proper operation and performance of the modem itself and for surrounding equipment.

Two aspects of noise in an OEM board design containing the modem device set must be considered: on-board/off-board generated noise that can affect analog signal levels and analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC), and on-board generated noise that can radiate off-board. Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality, especially in low level analog signals. Of particular concern is noise in frequency ranges affecting modem performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met to allow use in specific environments.

Proper PC board layout (component placement, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to attain EMI certification.

All the aspects of proper engineering practices are beyond the scope of this designer's guide. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

8.1 PC Board Layout Guidelines

1. Provide an adequate ground.
    a. In a 2-layer design, provide a ground grid in all unused space around and under components (judiciously near analog components) on both sides of the board and connect in such a manner as to avoid small islands. A grid is preferred over a plane to improve solderability. Typically, the grid is composed of .012 in. traces and .012 in. spaces on a .025 in. grid. Connect each grid to other grids on the same side at several points and to grids on the opposite side through the board at several points. Connect all modem DGND and AGND pins to the ground grid.
    b. In a 4-layer design, provide a ground plane covering the entire board. Connect all modem DGND and AGND pins to the ground plane at a single point.
2. As a general rule, route digital signals on the component side of the PCB and the analog signals on the solder side. The sides may be reversed to match particular OEM requirements. Route the digital traces perpendicular to the analog traces to minimize signal cross coupling.
3. Route the modem signals to provide maximum isolation between noise sources and noise sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The modem noise source, neutral, and noise sensitive pins are listed in Table 8-1.
4. All power and ground traces should be at least 0.05 inch wide.
5. Keep all traces and component leads connected to crystal input and output pins (e.g., XTLI and XTLO) short in order to reduce induced noise levels and minimize any stray capacitance that could affect the crystal oscillator. Keep the XTLO trace extremely short with no bends greater than 45 degrees and containing no vias since the XTLO pin is connected to a fast rise time, high current driver.
6. Connect crystal can(s) to ground.
7. Locate the modem device(s) and all supporting analog circuitry, including the data access arrangement, on the same area of the PCB.
8. Locate the analog components close to and on the side of board containing the TXA1, TXA2, and RIN signals.
9. Avoid placing noisy components and traces near TXA1, TXA2, RIN, VC, and VREF lines.
10. Locate receivers and drivers for DTE EIA-232 serial interface signals close to the connectors and away from traces carrying high frequency clocks in order to avoid/minimize the addition of noise suppression components (i.e., chokes and capacitors) for each line.
11. Route modem interconnect signals (e.g., TMODE to RMODE or ~IRQ to DSP_IRQ) directly to the interfacing by the shortest possible route avoiding all analog components.
12. Provide an RC network on the +5VA supply in the immediate proximity of the +5VA pin to filter out high frequency noise above 115 kHz. A tantalum capacitor is recommended (especially in a 2-layer board design) for improved noise immunity with a current limiting series resistor or inductor to the +5V supply which meets the RC filter frequency requirements.

13. Provide a 0.1 µF ceramic decoupling capacitor to ground between the high frequency filter and the +5VA pin.
14. Provide a 0.1 µF ceramic decoupling capacitor to ground between the +5V supply and the +5VD pin.

Table 8-1. Modem Pin Noise Characteristics

Function	Noise Source	Neutral	Noise Sensitive
VDD, VAA		11, 21, 36, 41, 56	
GND, DGND, AGND		10, 19, 22, 30, 40, 43, 55	
Crystal	12-13		
Control			
Eye Pattern	46-47, 53	48	
Line Interface		6, 28, 31	23, 26-27
Speaker Interface	29		
Serial/LED Interface	35, 50, 52, 54, 57	5, 7, 34, 37, 51, 58	
MCU Interface	9, 14-18, 20, 60-68	8, 59	
MDP Interconnect	3, 33, 42, 44-45, 49	2, 4, 24-25, 32 , 38-39	
No connection (NC)		1	

8.2 Electromagnetic Interference (EMI) Considerations

The following guidelines are offered to specifically help minimize EMI generation. Some of these guidelines are redundant with, or similar to, the general guidelines but are mentioned again to reinforce their importance.

In order to minimize the contribution of the modem device set-based design to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

These guidelines assume a microcontroller unit (MCU) is connected to the modem data pump (MDP).

Crystal Circuit

1. Place the crystal and related components as close as possible to the MCU and MDP devices, and in particular, the XTLI and XTLO pins.
2. For MCU and MDP devices that do not have an internal series resistor in the crystal circuit, place a 100-ohm (typical) resistor between the XTLO pin and the crystal/capacitor node.
3. Connect crystal capacitor ground connections directly to GND pin on the MCU and MDP devices. Do not use common ground plane or ground trace to route the capacitor GND pin to the corresponding MCU or MDP GND pin.

Digital Components

1. Place digital components close together in order to minimize signal trace length.
2. Use decoupling capacitors (0.1 µF) on each digital component.
3. Place one large 10 µF tantalum capacitor between power and ground near digital components.

Circuit Traces

1. Avoid right angle (90 degree) turns on high frequency traces. Use smoothed radiuses or 45 degree corners.
2. Minimize the number of through-hole connections (feedthroughs) on traces carrying high frequency signals.
3. Keep all signal traces away from crystal circuits.
4. Keep digital signals, EIA/TIA-232 signals, and DAA signals separated from each other.
5. Provide a good ground plane or grid. In some cases, a multilayer board may be required with full layers for ground and power distribution.
6. Eliminate ground loops, which are unexpected current return paths to the power source.
7. Locate high frequency circuits in a separate area to minimize capacitive coupling to other circuits.
8. Locate cables and connectors so as to avoid coupling from high frequency circuits.
9. Lay out the highest frequency signal traces next to the ground grid.
10. If a multilayer board design is used, make no cuts in the ground or power planes and be sure the ground plane covers all traces.

11. On 2-layer boards with no ground grid, provide a shadow ground trace on the opposite side of the board to traces carrying high frequency signals. This will be effective as a high frequency ground return if it is three times the width of the signal traces.
12. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.

Signal Conditioning

1. Keep traces carrying high frequency signals as short as possible.
2. Condition high frequency, long trace, and digital signals by inserting a series resistor (300 ohm typical) in the signal source.
3. Conditioning the ~READ signal alone may provide adequate EMI reduction.
4. Conditioning the address or data lines might also be necessary.

EIA/TIA-232 Interface Components

1. Place components close to each other and close to the EIA/TIA-232 interface cable connector.
2. Connect power and ground for all RS-232 components to the power and ground source points via separate power and ground traces that are not connected to the digital power and ground "except" at these source points. Power and ground source points are the board input pins or a regulator output if used.
3. Connect RS-232 cable signal ground wire to the ground source point.
4. Connect the EIA/TIA-232 cable shield ground to the ground source point.

Telephone and Local Hand Set Interface

1. Place common mode chokes in series with Tip and Ring for each connector.
2. Decouple the telephone line cables at the telephone line jacks. Typically, use a combination of series inductors, common mode chokes, and shunt capacitors. Methods to decouple telephone lines are similar to decoupling power lines, however, telephone line decoupling may be more difficult and deserves additional attention. A commonly used design aid is to place footprints for these components and populate as necessary during performance/EMI testing and certification.
3. Place high voltage filter capacitors (.001 µF @1KV) from Tip and Ring to Ground.

Stand Alone Modem Chassis

1. Use a metal enclosure.
2. If a plastic enclosure is required, internal metal foil lining the enclosure or conductive spray applied to the top and bottom covers may reduce emissions.

Power and Ground

1. Keep the current paths of separate board functions isolated, thereby reducing the current's travel distance. Separate board functions are: host interface, display, digital (SRAM, EPROM, MCU, MDP), and DAA. Power and ground for each of these functions should be separate islands connected together at the power and ground source points only.
2. Do not place ground or voltage planes beneath the telephone line side of the Tip and Ring chokes.
3. Decouple power from ground with decoupling capacitors as close to the modem device power pins as possible.
4. Decouple the power cord at the power cord interface with decoupling capacitors. Methods to decouple power lines are similar to decoupling telephone lines.

Optional Configurations

Because fixed requirements of a design may alter EMI performance, guidelines that work in one case may deliver little or no performance enhancement in another. Initial board design should, therefore, include flexibility to allow evaluation of optional configurations. These optional configurations may include:

1. Chokes in Tip and Ring lines replaced with jumper wires as a cost reduction if the design has sufficient EMI margin.
2. Various grounding areas connected by tie points (these tie points can be short jumper wires, solder bridges between close traces, etc.).
3. EIA/TIA-232 cable ground wire or cable shielding connected on the board or floated.
4. Two designs in parallel with one based on a two layer board and the other based on a four layer board. During the evaluation phase, better performance of one design over another may result in quicker time to market.

8.3 Crystal Specifications

The specifications and recommended suppliers for crystals are listed in Table 8-2.

Table 8-2. Crystal Specifications - 52.416 MHz

Characteristic	Value	Value
Rockwell Part No.	333R45-008	5333R04-013
Electrical		
Frequency	52.416 MHz nom.	52.416 MHz nom.
Frequency Tolerance	±40 ppm (C_L = 16.5 and 19.5 pF)	±50 ppm (C_L = 16.5 and 19.5 pF)
Frequency Stability		
vs. Temperature	±45 ppm (0°C to 70°C)	±35 ppm (0°C to 70°C)
vs. Aging	±15 ppm/5 years	±15 ppm/4 years
Oscillation Mode	Third overtone	Third overtone
Calibration Mode	Parallel resonant	Parallel resonant
Load Capacitance, C_L	18 pF nom.	18 pF nom.
Shunt Capacitance, C_O	6 pF max.	7 pF max.
Series Resistance, R_1	35 Ω max. @20 nW drive level	80 Ω max. @20 nW drive level
Drive Level	100µW correlation; 500µW max.	100µW correlation; 300µW max.
Operating Temperature	0°C to 70°C	0°C to 70°C
Storage Temperature	–40°C to 85°C	–30°C to 80°C
Mechanical		
Dimensions (L x W x H)	11.05 x 4.65 x 13.46 mm	7.5 x 5.2 x 1.3 mm (max.)
Mounting	Through Hole	SMT
Holder Type	HC-49/U	
Suggested Suppliers		
	KDS America Toyocom U.S.A., Inc. Hy-Q International (USA), Inc. Vectron Technologies, Inc.	KDS America Hy-Q International (USA), Inc. Vectron Technologies, Inc.

Notes

1. Characteristics @ 25°C unless otherwise noted.
2. Supplier Information:

KDS America
Fountain Valley, CA
(714) 557-7833

Toyocom U.S.A., Inc.
Costa Mesa, CA
(714) 668-9081

Hy-Q International (USA), Inc.
Enlanger, KY
(606) 283-5000

Vectron Technologies, Inc.
Lowell, NH
(603) 598-0074

8.4 RECOMMENDED INTERFACE CIRCUITS

The recommended interface connections to the modem are shown in Figure 8-1 (68-pin PLCC),

A typical external circuit for connection to the line with no external hybrid and a transmit level to -7 dBm is shown in Figure 8-2.

A typical external circuit for connection to the line with an external hybrid and a transmit level to 0 dBm is shown in Figure 8-3.

A typical external speaker circuit is shown in Figure 8-4.

An eye pattern generator circuit is shown in Figure 8-5.

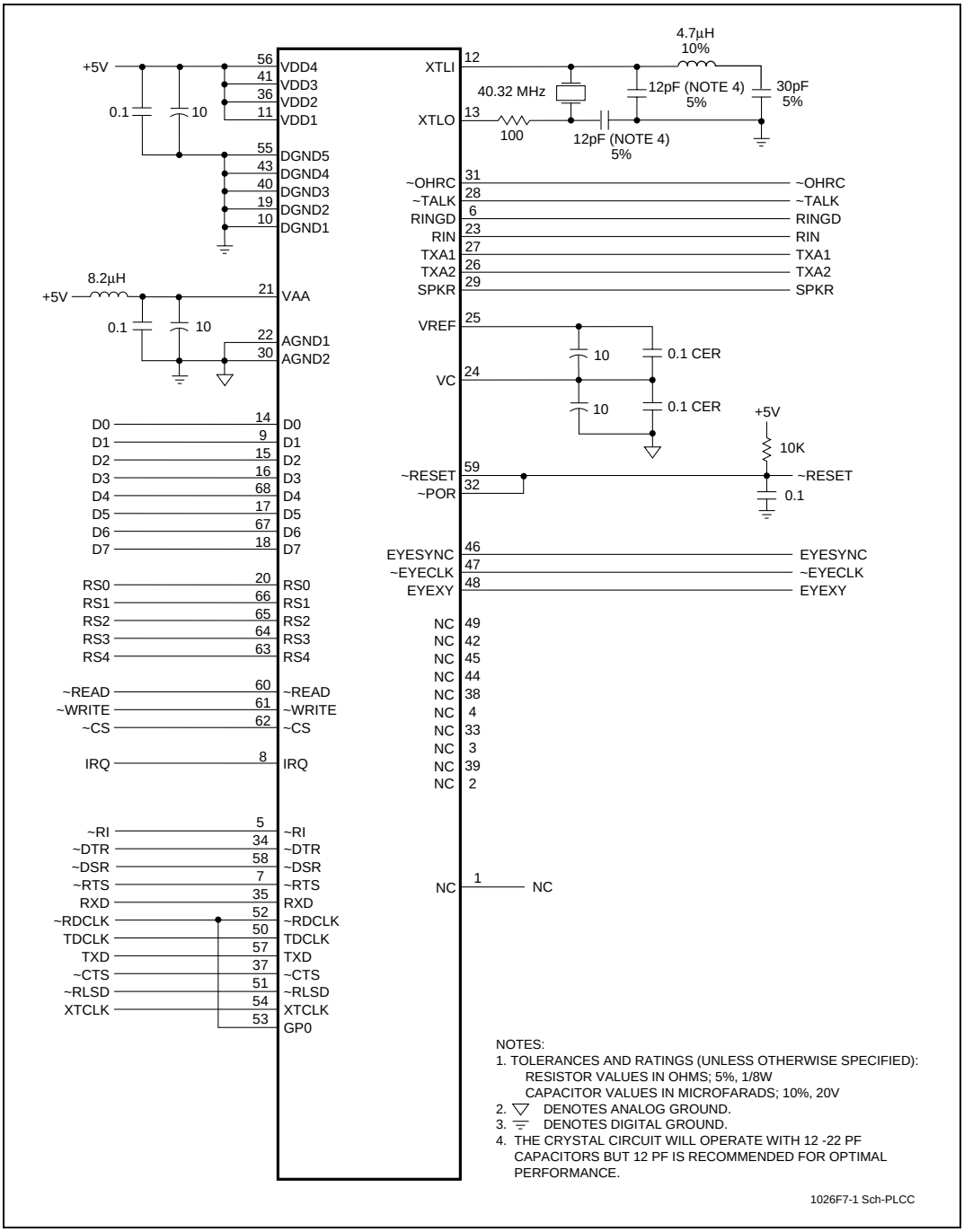


Figure 8-1. Interface Schematic - 68-Pin PLCC

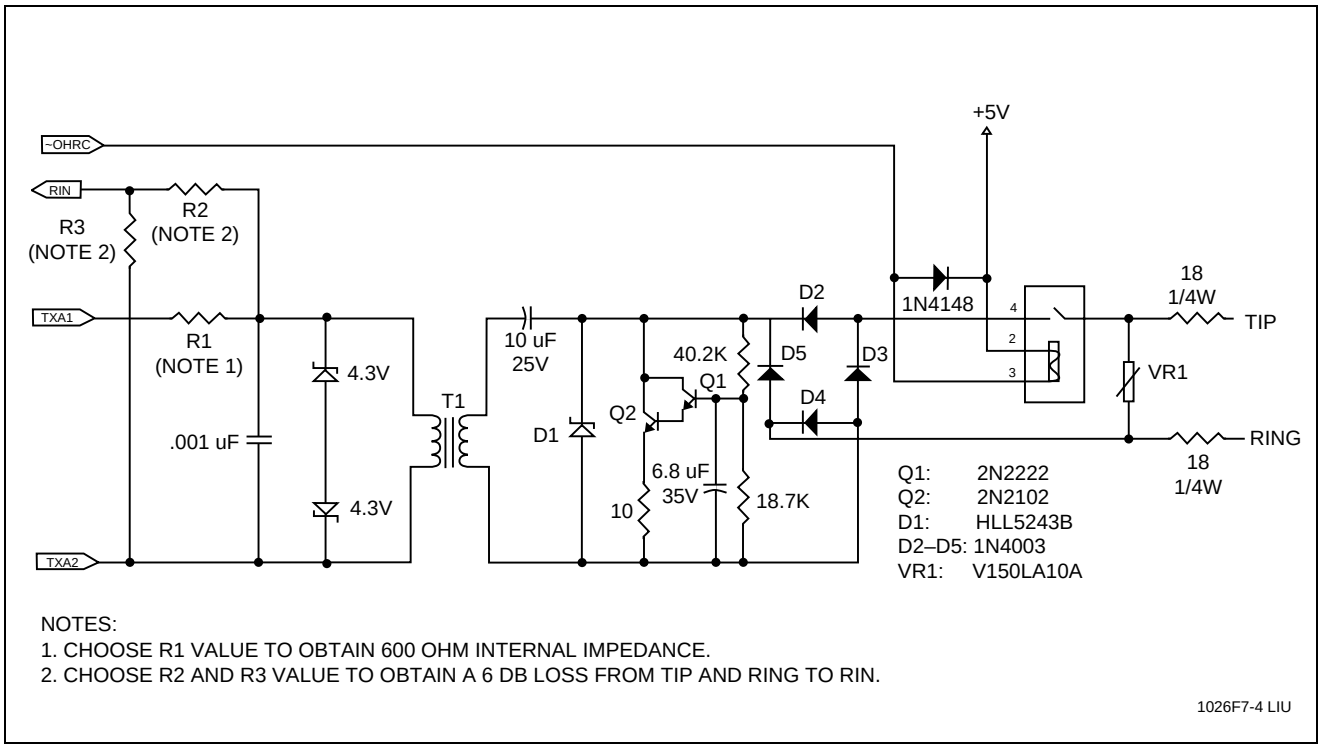


Figure 8-2. Typical Line Interface

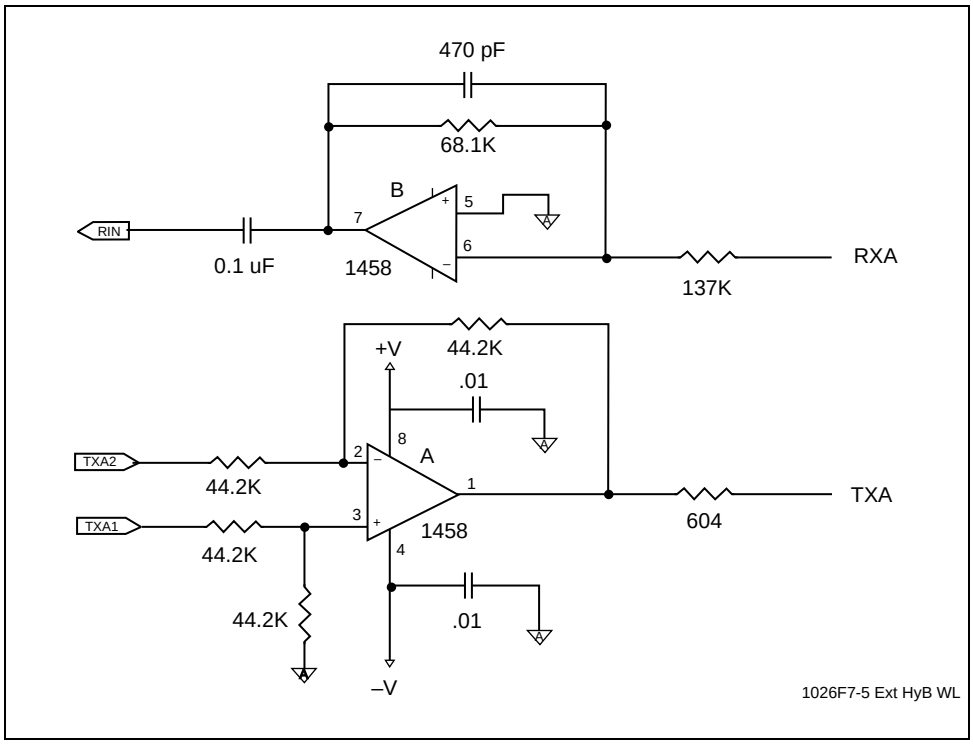


Figure 8-3. Typical Interface to External Hybrid

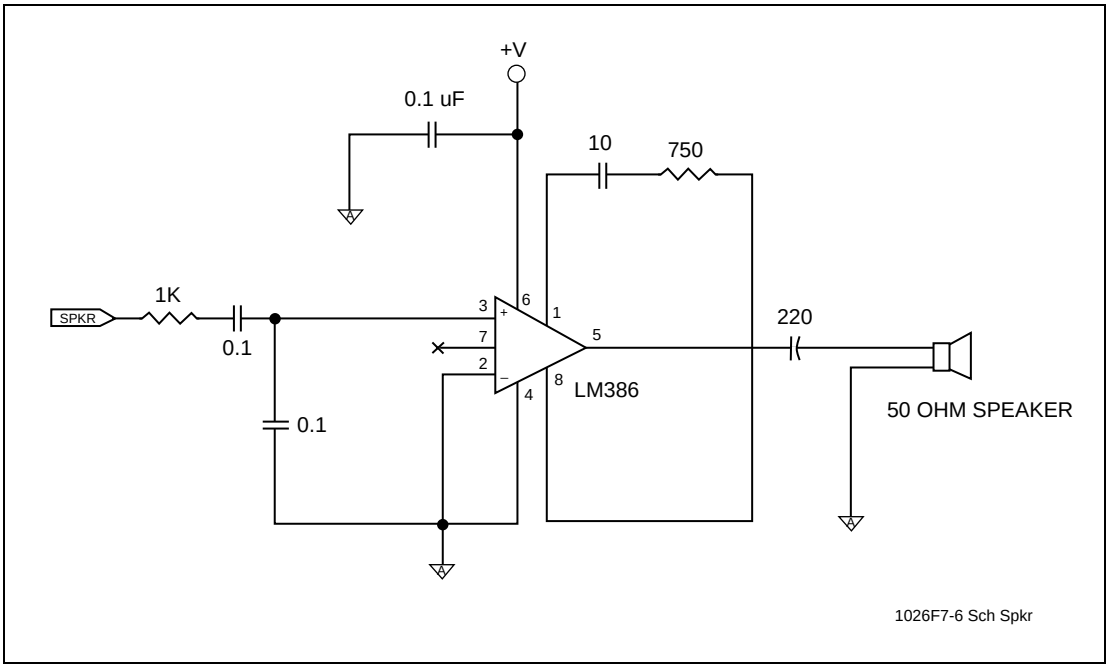


Figure 8-4. Typical External Speaker Circuit

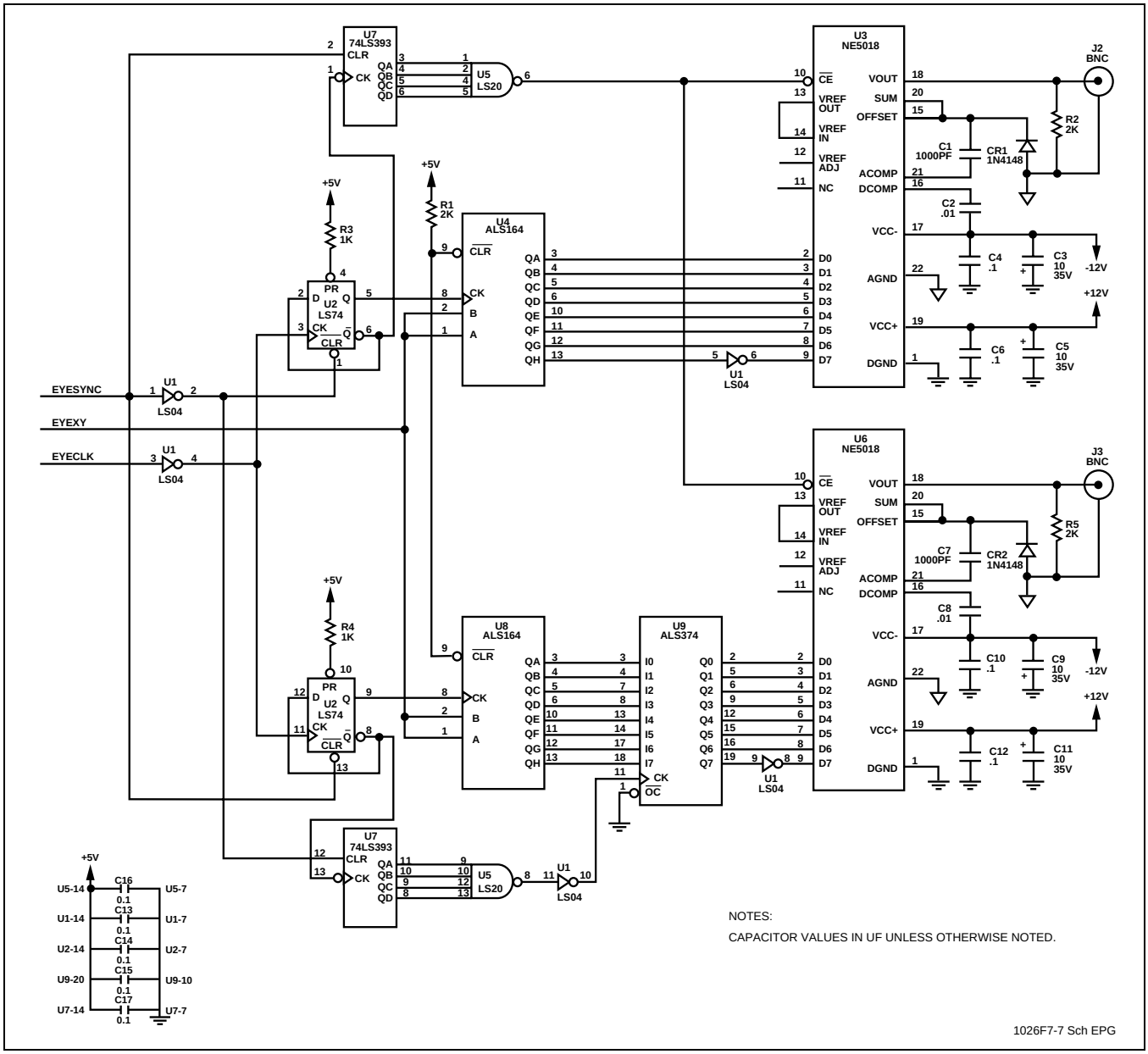


Figure 8-5. Eye Pattern Generator Circuit

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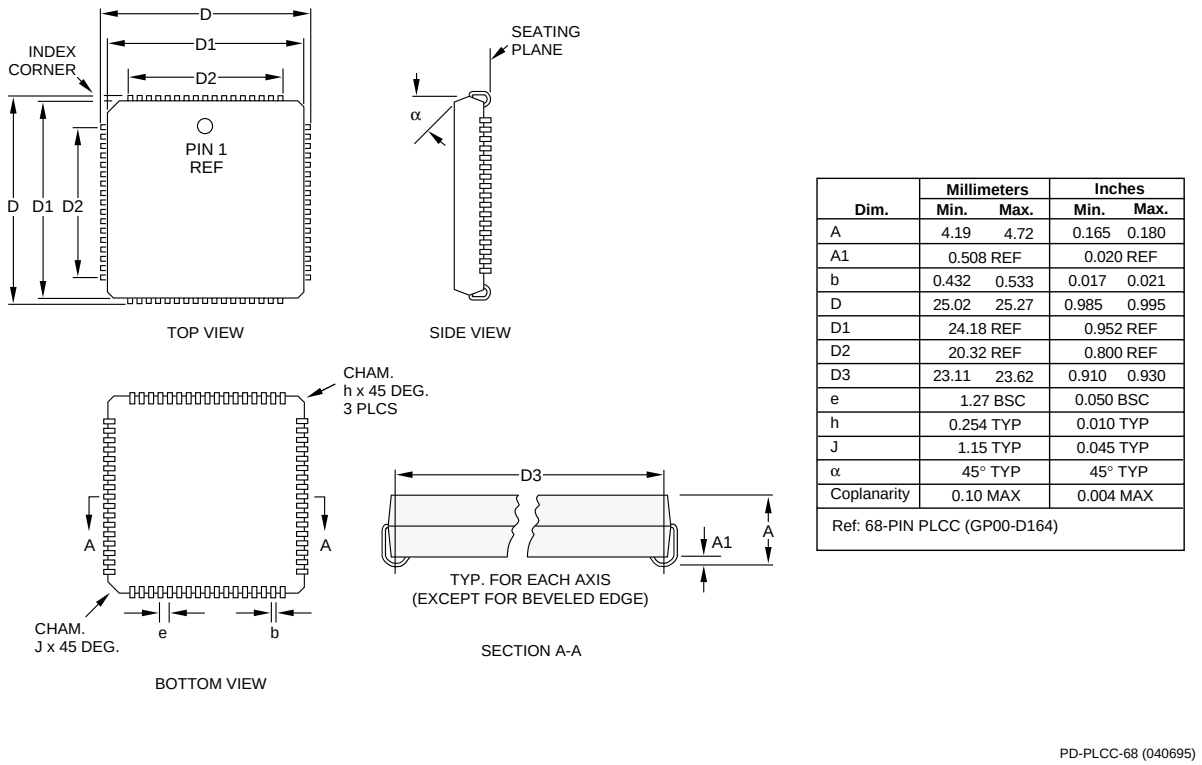
9. PACKAGE DIMENSIONS

The package dimensions are shown in Figure 9-1.



Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	4.19	4.72	0.165	0.180
A1	0.508 REF		0.020 REF	
b	0.432	0.533	0.017	0.021
D	25.02	25.27	0.985	0.995
D1	24.18 REF		0.952 REF	
D2	20.32 REF		0.800 REF	
D3	23.11	23.62	0.910	0.930
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
Coplanarity	0.10 MAX		0.004 MAX	
Ref: 68-PIN PLCC (GP00-D164)				

Figure 9-1. Package Dimensions - 68-Pin PLCC

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INSIDE BACK COVER NOTES

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